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Comparative Evaluation of ARCP and Three-Level TCM Soft-Switching Bridge-Legs for High-Frequency SiC Converter Systems

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***Abstract*—Soft-switching bridge-legs facilitate high-efficiency three-phase PV inverters or PFC rectifiers. By extending a half-bridge with a resonant auxiliary circuit, including two additional transistors, zero-voltage switching (ZVS) of the main transistors can be realized (Active Resonant Commutated Pole, ARCP). Alternatively, a similar T-type bridge-leg structure achieves ZVS by operating the output filter inductor with a sufficiently high current ripple (with 3-level Triangular Current Modulation, 3L-TCM). We provide a comparative evaluation of these two concepts for the realization of 2.2 kW (per phase), 800 V DC bridge-legs with latest-generation 1200 V and 650 V SiC MOSFETs, discussing chip-area optimization, filter design for compliance with current and future EMI limits, and qualitative limits and design criteria. The calculated loss-vs.-volume Pareto fronts indicate advantages for the 3L-TCM approach, with peak switching frequencies of 72 kHz or 144 kHz and an efficiency (semiconductors and EMI filter) of about 99.6 %. The ARCP concept seems more suitable for applications that do not necessarily require EMI filters but benefit from limited switch-node dv/dt (in the order of 1.5 V/ns) such as variable-speed drives.**

I. Introduction

Grid-connected three-phase voltage DC-link converters such as PFC rectifiers and PV inverters, which we consider for the presented analysis, must employ input/output filters to allow a connection to the mains and to ensure electromagnetic compatibility (EMC). Similarly, variable-speed motor drive systems (VSDs) for the automation industry or robotics would ideally employ three-phase DC-AC inverter stages with LC output filters to prevent conducted common-mode (CM) and radiated emissions of motor cables, $\mathrm{d}v/\mathrm{d}t$ motor winding stress, reflections on long motor cables, and motor bearing currents. To obtain a small filter volume, advantageously a high switching frequency and, for guaranteeing high efficiency, soft-switching should be used. Both aspects can be covered using two-level bridge-legs and wide-bandgap (WBG) power semiconductors with auxiliary circuitry for achieving soft-switching, a so called Auxiliary Resonant Commutated Pole (ARCP), as depicted in **Fig. 1(a)**, where only a single bridge-leg of a three-phase inverter is shown. This concept has been proposed for the reduction of bipolar transistor switching losses in 1983 [1], and has later been extensively analyzed, e.g., in [2]–[5]. Recently, it has been reconsidered for high-power automotive inverters [6] and a low-power GaN-based inverter for VSDs [7]. This soft-switching concept utilizes a current in the inductor L_r to charge/discharge the capacitors C_r placed in parallel to the bridge-leg's main switches $\mathrm{T_{p,h}}$ and $\mathrm{T_{p,l}}$ during the interlock delay time. This facilitates zero-voltage switching (ZVS) of the main switches and therefore renders the switch-node's voltage transitions $-V_\mathrm{dc}/2 \rightarrow V_\mathrm{dc}/2$ and $V_\mathrm{dc} \rightarrow -V_\mathrm{dc}/2$ ideally lossless, regardless of the direction of i_L1. The ARCP requires auxiliary circuit elements in addition to the bridge-leg's transistors and the output filter, i.e., the two transistors $\mathrm{T_{p,l}}$ and $\mathrm{T_{n,h}}$, the inductor L_r, and the two capacitors $C_\mathrm{r,p} = C_\mathrm{r,n} = C_\mathrm{r}/2$. **Fig. 1(c)** shows characteristic current waveforms for a single fundamental period of the output current.

By using the same number of power semiconductors as in an ARCP bride-leg, soft-switching can also be realized without the additional passive components by so-called 3-level Triangular-Current-Mode (3L-TCM) operation [8]–[13], as depicted in **Fig. 1(b)**. According to the large inductor current ripple (see **Fig. 1(d)**), the filter inductance value/volume is minimized and the local reversal of the current flow direction at the end of each pulse interval is utilized to achieve ZVS of all power semiconductors. Even though the current ripple is large, the power transistor conduction losses increase only by about 30 % compared to a purely sinusoidal (fundamental-frequency) current [14]. Also, only a current zero-crossing-detection (ZCD) circuit but no full current sensor needs to be employed. Due to the connection of the filter capacitors to the midpoint m of the DC bus (or, alternatively, to the negative rail), the differential-mode (DM) and the CM switching frequency components are simultaneously attenuated, i.e., a phase-modular structure of a three-phase inverter results. Note that as the bridge-leg generates a sinusoidal voltage with reference to the DC midpoint, the switching frequency resulting around the current zero crossing (assuming close to zero phase shift between the output current and the output voltage) approaches zero.

The above mentioned concepts for soft-switching bride-legs are highly interesting for the realization of future VSDs, PFC rectifiers, and high-efficiency PV inverter systems. However, whereas they have been individually analyzed in the literature, a comparison considering latest WBG power semiconductor technology as well as upcoming EMI standards for an extended frequency range from 150 kHz down to 9 kHz is missing, which motivates the analysis described in this paper.

II. EMI Filter Desgin

The analyzed ARCP and 3L-TCM bridge-legs (see **Fig. 1(a),(b)** and **Tab. I** for the considered specifications) achieve soft-switching using conceptually different approaches. Like a conventional two-level half-bridge, the ARCP bridge-

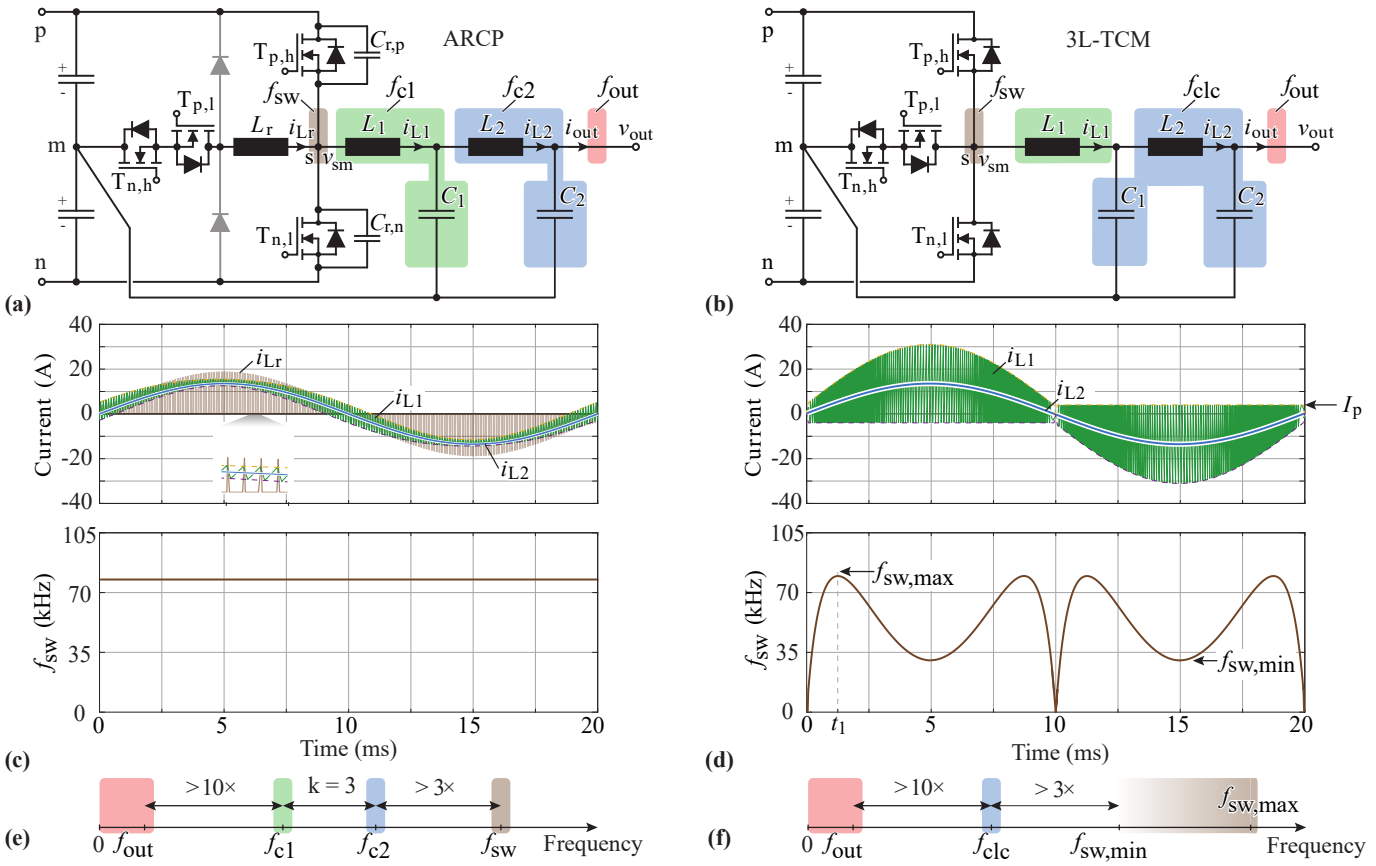

Fig. 1. (a,b) ARCP and 3L-TCM bridge-legs with two-stage output filter. **(c)** ARCP current waveforms for f_{sw} = 72 kHz, L_1 = 342 µH, L_r = 16 µH, and $C_{r,p} = C_{r,n}$ = 2.2 nF. **(d)** 3L-TCM current and switching frequency waveforms (low-frequency filter capacitor current neglected) for L_1 = 83 µH. **(e,f)** Assumed frequency separation conditions that should be fulfilled by the output filter designs.

TABLE I
BRIDGE-LEG SPECIFICATIONS.

Parameter	Symbol	Value	Unit
DC-link voltage	V_{dc}	800	V
Output voltage amplitude	$\hat{V}_{out}$	$230\sqrt{2}$	V
Nominal output power	P_{out}	2.2	kW
Output electrical freq.	f_{out}	50	Hz

leg operates with a constant switching frequency. However, the ARCP renders the otherwise hard-switching transitions ideally lossless by the action of the auxiliary circuitry (switches $T_{p,l}$, $T_{n,h}$ and passive components L_r, $C_{r,p}$, $C_{r,n}$), i.e., achieves soft-switching. In contrast, the 3L-TCM achieves soft-switching by means of a large current ripple in the first-stage filter indcutor L_1, whose envelope[1] is shown in in **Fig. 1(d)** together with the resulting varying switching frequency. Therefore, the spectra of the two concept's switch-node voltages v_{sm} differ as can be seen in **Fig. 2**. The ARCP spectrum shows the characteristic peaks located at multiples of the switching frequency f_{sw} (e.g., 72 kHz), whereas the 3L-TCM spectrum is spread out between $f_{sw,min}$ and $f_{sw,max}$ (e.g., between 23.4 kHz and 72 kHz). In grid-connected applications, the output voltage v_{out} must comply with EMI standards (see the limits in **Fig. 2**). Therefore, the bridge-legs must be extended by two-stage EMI filters formed by L_1C_1-L_2C_2 to attenuate the high-frequency (HF) noise components of v_{sm} to values sufficiently below the limits given by the standard. In general, the thus required attenuation (in dBµV) is

$$\mathrm{Att}_{req}(f) = \mathrm{EMI}_{limit}(f) - \mathrm{QP}_{max}(f) - \mathrm{EMI}_{margin}(f), \quad (1)$$

where $\mathrm{EMI}_{limit}(f)$ is determined by the standard (see **Fig. 2**), $\mathrm{QP}_{max}(f)$ is the calculated maximum QP approximation [15] of the unfiltered noise emissions, and EMI_{margin} = 10 dBµV accounts for component tolerances.

A. Filter Design for ARCP Bridge-Legs

The constant switching frequency operation of the ARCP allows to use the filter design approach known for conventional hard-switched two-level inverters, where the filter cutoff frequencies $f_{c1} = 1/(2\pi\sqrt{L_1C_1})$ and $f_{c2} = 1/(2\pi\sqrt{L_2C_2})$ are typically placed in the frequency spectrum as depicted in **Fig. 1(e)**. These criteria ensure that the filter does not interact with the fundamental frequency f_{out} (leaving some control margin) and with the switching frequency f_{sw}. The condition $f_{c1} > 10 f_{out}$ is easily fulfilled in the analyzed PV inverter application with f_{out} = 50 Hz, but would become more relevant in motor drive applications where f_{out} can reach > 250 Hz, and where additional control-bandwidth-related considerations may apply. We consider passive damping of the second filter

[1]Note that the inductor current changes sign in each switching period, which facilitates ZVS for all transistors.

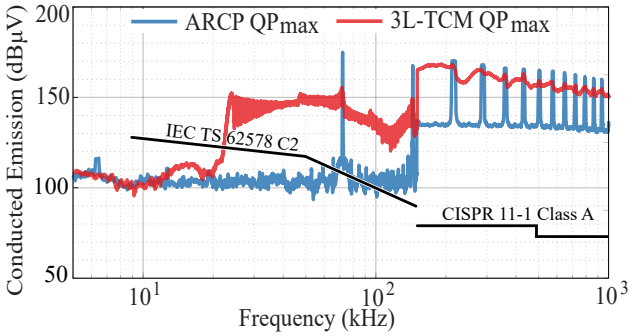

Fig. 2. Simulated noise emissions (maximum quasi-peak (QP) approximation [15]) without any EMI filter of the ARCP and the 3L-TCM bridge-legs at the nominal operating point and for $f_{sw} = f_{sw,max} = 72\,\text{kHz}$, respectively. Also shown are the QP limits given in CISPR 11-1-A [16] (in force) and upcoming limits for the lower frequency range from 9 kHz to 150 kHz as proposed in the IEC TS 62578 C2 [17].

stage[2] (optimum parallel L_{d2}-R_{d2} damping with $L_{2d} = n \cdot L_2$ and $n = 1$, see [18]) and account for the corresponding degradation of the high-frequency attenuation by adding 6 dB to $\text{EMI}_{\text{margin}}$. Note that the switching frequency f_{sw} is separated from the filters' resonant frequencies f_{c1} and f_{c2}, which ensures low losses in the damping network. The output filter transfer function can be approximated by linear segments in a double-logarithmic scale, i.e., 0 dB per decade for frequencies $< f_{c1}$, −40 dB per decade for frequencies between f_{c1} and f_{c2} and −80 dB per decade for frequencies hihger then f_{c2}. This assumption allows to analytically calculate the filter cutoff frequencies from the required attenuation as

$$f_{c1} = \min\left(10^{\text{Att}_{\text{req}}(f)/80} \cdot \frac{f}{\sqrt{k}}\right), \tag{2}$$

where the factor $k = 3$ represents the ratio of the two cutoff frequencies, i.e., $f_{c2} = k\, f_{c1}$.

The first-stage filter inductor L_1 is chosen such that the maximum high-frequency i_{L1} single-side ripple amplitude is limited to 30 % of the output current amplitude, i.e.,

$$L_1 = \frac{V_{dc}}{4 \cdot \Delta I_{L,p2p} \cdot f_{sw}}, \tag{3}$$

where $\Delta I_{L,p2p} = 2 \cdot 0.3 \cdot \hat{I}_{out} = 8.1\,\text{A}$ and $\hat{I}_{out} = 13.5\,\text{A}$.

The filter capacitor values C_1 and C_2 are chosen such that the total filter capacitance is equal to $C_1 + C_2 = C_{max}$, where $C_{max} = 2Q_{c,max}/(\hat{V}_{out}^2 \omega_{out,max}) = 13.2\,\mu\text{F}$ follows from the maximum allowable reactive power consumption of 10 % of the output power, i.e., $Q_{c,max} = 0.1 P_{out} = 0.22\,\text{kVAr}$. It is then straightforward to obtain the capacitor values for the first and the second filter stages as $C_1 = 1/(\omega_{c1}^2 L_1)$ and $C_2 = C_{max} - C_1$, where $\omega_{c1} = 2\pi f_{c1}$. No design (for the considered switching frequency) is possible if $C_2 < 0$ results. Finally, L_2 follows as $L_2 = 1/(\omega_{c2}^2 C_2)$ with $\omega_{c2} = 2\pi f_{c2}$.

The outlined procedure is used to obtain filter designs for ARCP bridge-legs operating with the three different switching frequencies (48 kHz, 72 kHz and 144 kHz), which are listed in **Tab. II** (considering only the CISPR 11 Class A [16] EMI standard) and in **Tab. III** (considering also the limits for the lower frequency range of 9 kHz to 150 kHz proposed in IEC TS 62578 [17]). Note that the current-ripple criteria (3) forces rather large values for L_1 and consequently leaves the second-stage inductor L_2 much smaller.

[2]In a two-stage output filter as depicted in **Fig. 1(a)**, the inductor current i_{L1} is typically controlled in a closed-loop fashion, allowing to actively damp eventual oscillations between L_1 and C_1.

TABLE II
CHOSEN FILTER PARAMETERS FOR $f_{out} = 50\,\text{Hz}$ COMPLIANT WITH CISPR11-1-A.

$f_{sw}/f_{sw,max}$ (kHz)	L_1 (µH)	C_1 (µF)	f_{c1}/f_{clc} (kHz)	L_2 (µH)	C_2 (µF)	f_{c2} (kHz)	R_{2d} (Ω)
ARCP							
48	513	1.8	5.3	8.7	11.5	15.9	1.3
72	342	2.4	5.6	8.2	10.9	16.8	1.3
144	171	3.1	6.9	5.9	10.1	20.7	1.1
3L-TCM							
48	135	6.6	4.9	320	6.6	–	10.1
72	83	6.6	7.8	126	6.6	–	6.3
144	36	6.6	7.2	150	6.6	–	6.9

TABLE III
CHOSEN FILTER PARAMETERS FOR $f_{out} = 50\,\text{Hz}$ COMPLIANT WITH IEC TS 62578 AND CISPR11-1-A.

$f_{sw}/f_{sw,max}$ (kHz)	L_1 (µH)	C_1 (µF)	f_{c1}/f_{clc} (kHz)	L_2 (µH)	C_2 (µF)	f_{c2} (kHz)	R_{2d} (Ω)
ARCP							
48	513	4.3	3.4	27.1	9.0	10.2	2.5
72	342	5.0	3.9	22.7	8.3	11.6	2.4
144	171	7.0	4.6	21.1	6.3	13.8	2.7
3L-TCM							
48	135	6.6	4.5	380	6.6	–	11.0
72	83	6.6	7.8	126	6.6	–	6.3
144	36	6.6	7.2	150	6.6	–	6.9

B. Filter Design for 3L-TCM Bridge-Legs

A 3L-TCM bridge-leg uses a large HF current ripple in i_{L1} to achieve soft-switching, which results in the current envelope depicted in **Fig. 1(d)**. Consequently, the switching action occurs once i_{L1} reaches the envelope's minimum/maximum. Therefore, and neglecting resonant intervals, the i_{L1} current envelope commands the switching actions of the 3L-TCM bridge-leg; in practice a zero-current detection (ZCD) circuitry is used to provide feedback, i.e., ultimately a closed-loop tolerance-band-like current control results. As shown in **Fig. 3**, the 3L-TCM bridge-leg together with the inductor L_1 thus behaves like a current source towards the two-stage filter's remaining CLC-part (C_1-L_2-C_2), which is advantageous regarding the EMI filter design (see below).

The choice of L_1 is very important as it, besides the current envelope, determines the maximum switching frequency (cf.

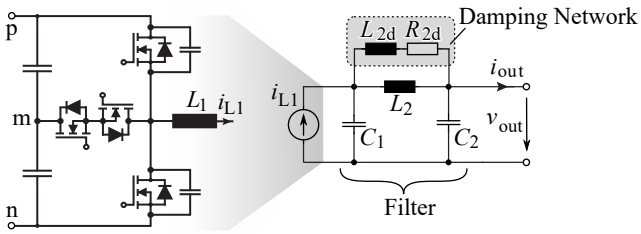

Fig. 3. The 3L-TCM bridge-leg including the inductor L_1 can be represented as current source, which facilitates the design of the remaining CLC filter structure.

Fig. 1(d)) reached within a fundamental AC period. It can be designed with

$$L_1 = \frac{V_{dc}}{4 f_{sw,max}} \cdot \frac{M \sin(\omega t_1) \cdot [1 - M \sin(\omega t_1)]}{\hat{I}_{out,nom} \sin(\omega t_1) + I_p}, \qquad (4)$$

where $M = 2\hat{V}_{out}/V_{dc} = 0.81$ is the modulation index and $\sin(\omega t)$ is the assumed time modulation function of the output voltage and current, i.e., $v_{out} = \hat{V}_{out} \sin(\omega t)$ and $i_{out} = \hat{I}_{out} \sin(\omega t)$. Note that for the considered type of TCM modulation the calculation of L_1 does not depend on the load, i.e., a nominal peak value of the output current $\hat{I}_{out,nom} = 13.5\,\text{A}$ is used in (4). The current ripple amplitude is kept constant for part-load operation such that the frequency variation, i.e., $f_{sw,min}$ and $f_{sw,max}$, does not change. Whereas this causes still relatively high losses in L_1 for lower load currents, the approach also results in a HF noise spectrum that is independent of the load, thus simplifying the EMI filter design. Alternative approaches to handling part-load operation, e.g., by widening the current envelope only locally as needed,[3] are subject of future analyses. The discharge current I_p in (4) is calculated using the effective switch-node capacitance and the energy condition necessary for guaranteeing soft-switching, cf. [14], [19]. The point in time when the maximum switching frequency is reached (t_1 in **Fig. 1(d)**) can be calculated from

$$\sin(\omega t_1) = \frac{\sqrt{I_p(\hat{I}_{out,nom} + M\, I_p)} - \sqrt{M}\, I_p}{\sqrt{M}\, \hat{I}_{out,nom}}. \qquad (5)$$

In the first step of the filter design, L_1 is determined from $f_{sw,max}$ using (4). Considering then the current-source approach depicted in **Fig. 3** facilitates a straightforward design of the remaining CLC filter structure. It can be shown that the C_1-L_2-C_2 filter achieves maximum attenuation when $C_1 = C_2$ for a given L_2. Therefore, determining the filter capacitances is straightforward as the maximum allowable capacitance $C_{max} = 13.2\,\mu\text{F}$ is given from the reactive power limit (see above). The first filter capacitor takes the larger value of either $C_1 = C_{max}/2$ or $C_1 = (\hat{I}_{out,nom} + I_p)/(\omega_{sw,min} \cdot 0.1\,\hat{V}_{out})$ which limits the HF voltage ripple (fundamental-switching-frequency approximation) of C_1 to max. 10 % of the output voltage amplitude $\hat{V}_{out}$, and $C_2 = C_{max} - C_1$. The inductor value L_2 then follows from the required resonance frequency of the CLC filter's $v_{out}(s)/i_{L1}(s)$ transfer function, which is $f_{clc} = 1/(2\pi\sqrt{C_{12}\, L_2})$ with $C_{12} = C_1 C_2/(C_1 + C_2)$. f_{clc} must be low enough to provide the required attenuation to meet the EMI regulations (considering the same margins as discussed above), and in addition we require a spectral separation of f_{clc} and $f_{sw,min}$ as $f_{clc} < f_{sw,min}/3$ (to prevent excessive losses in the passive damping circuit). Accordingly, the CLC filter's resonant frequency f_{clc} is limited either by EMI standards or by the 3L-TCM bridge-leg's minimum switching frequency.

As depicted in **Fig. 2**, the 3L-TCM spectrum is spread between $f_{sw,min}$ and $f_{sw,max}$, therefore, knowing the conventional EMI standard limits starting at 150 kHz, it is reasonable to chose the same $f_{sw,max}$ values as for the f_{sw} of the ARCP bridge-leg, i.e., 48 kHz, 72 kHz and 144 kHz. The thus designed filter values are shown in **Tab. II** (considering only the CISPR 11 Class A [16] EMI standard) and in **Tab. III** (also considering the limits for the lower frequency range of 9 kHz to 150 kHz proposed in IEC TS 62578 [17] as well). For $f_{sw,max} = 48\,\text{kHz}$ and $f_{sw,max} = 72\,\text{kHz}$, the filter resonant frequency is limited by the required spectral separation from the switching frequency, i.e., $f_{clc} = f_{sw,min}/2$, whereas for $f_{sw,max} = 144\,\text{kHz}$ the EMI limit defines f_{clc}.

[3]This would result in better part-load efficiency, but potentially adversely affect the EMI filter design due to the expected concentration of spectral energy around $f_{sw,max}$.

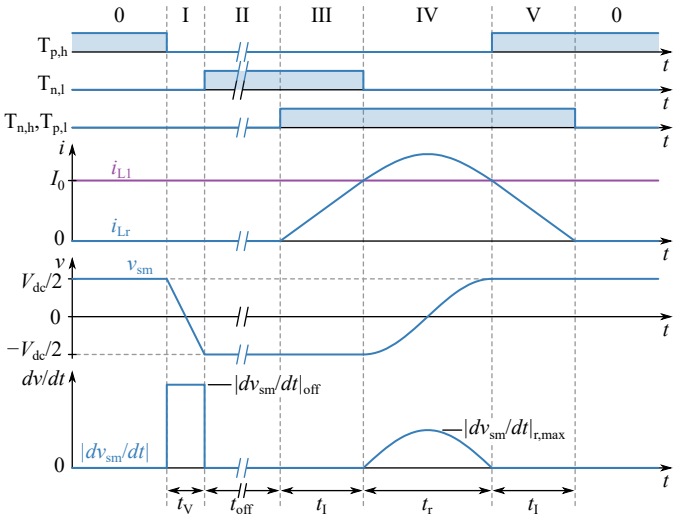

Fig. 4. Basic operating principle of the ARCP bridge-leg shown in **Fig. 1(a)**. Note that phase 0 and phase II are typically much longer than the other phases; they correspond to the states where the switch node is either connected to the positive or to the negative DC-link rail.

III. Implementation and Component Selection

With the design procedure outlined in the previous **Section II** defining the filter element values needed to comply with selected EMI standards, in a next step we investigate the implementation effort of both approaches, including characteristic features to obtain full soft-switching under all operating conditions and associated limitations. Then, we discuss the selection of suitable semiconductor devices and the design of all filter components, as well as corresponding loss models.

A. Implementation Aspects

1) ARCP: The ARCP bridge-leg employs additional passive components (L_r, $C_{r,p}$, $C_{r,n}$) to facilitate soft-switching of the main transistors for all operating conditions [1], [3], i.e., especially also for the otherwise hard-switched transition of the half-bridge (note that for a given output current direction the active turn-off transitions, i.e., where a MOSFET turn-off initiates the commutation to the complementary diode, are always soft-switched). To emphasize the implementation requirements and the design criteria of the ARCP's passive components, we briefly discuss the basic operating principle based on **Fig. 4**. A more detailed discussion is beyond the scope of this paper and can be found in the literature, e.g., in [3], [4].

Considering an operating point with positive output current $i_{L1} = I_0$, the high-side transistor $T_{p,h}$ is turned on during phase 0 and thus the switch node s connected to the positive DC-link potential p. When $T_{p,h}$ turns off, the load current charges/discharges the capacitors $C_{r,p}$ and $C_{r,n}$ with a

$(dv_{sm}/dt)_{off} = I_0/C_r$ (phase I) until $T_{n,l}$ can be turned on with zero applied voltage upon entering phase II, i.e., the part of a switching period where the switch node is connected to the negative DC-link potential n.

To initiate the switching transition in the other direction, the auxiliary transistors $T_{n,h}$ and/or $T_{p,l}$ are turned on (phase III), leading to a linear current build-up in the auxiliary inductor with $di_{Lr}/dt = 0.5V_{dc}/L_r$ until i_{Lr} reaches the output current level after $t_I = 2L_rI_0/V_{dc}$. This (i.e., $i_{Lr} = I_0$) marks the start of phase IV. As the current in the main transistor $T_{n,l}$ is then zero, it turns off in a soft transition (zero voltage and zero current). The following resonant transition of the switch-node potential from n to p is defined by L_r and C_r. Assuming lossless circuit elements and ideal conditions, the high-side main switch $T_{p,h}$ can be turned on with zero applied voltage and zero current after half the resonant period, i.e., $t_V = \pi\sqrt{L_rC_r}$.[4] During the subsequent phase V, L_r is demagnetized and the auxiliary transistors are turned-off once $i_{Lr} = 0$, giving rise to a (fast) resonant charging of their output capacitances (not shown for simplicity). To prevent oscillations, this last transient is then stopped by clamping diodes [20] (with an optional damping network) as shown (in gray) in **Fig. 1(a)**.

The resonant circuit elements L_r and C_r should ideally be small in value and thus size. However, this would lead to high di/dt and dv/dt, i.e., to fast transients and corresponding challenges regarding the ARCP control system implementation (sensing, timing), which thus in practice ultimately limits the maximum feasible dynamics (i.e., resonant frequency of the auxiliary network) [21]. We therefore select a maximum voltage slope of the resonant cycle of $|dv_{sm}/dt|_{r,max} = 1.5\,V/ns$, which can be related to the L_rC_r product as [22]

$$L_rC_r = \frac{V_{dc}^2}{4 \cdot |dv_{sm}/dt|_{r,max}^2}. \tag{6}$$

To limit the inductor current's maximum rate of change (during the linear ramp-up phase III) to 25 A/µs, we select $L_r = 16\,\mu H$ and find $C_r = 4.4\,nF$ with (6); this corresponds to 2.2 nF per main transistor, where, to simplify the control implementation, anyways a sufficiently large value is desirable to linearize (dominate) the MOSFET's non-linear output capacitances. With this design, the maximum dv/dt occurs during a turn-off transition (phase I) with the maxmium phase current $I_0 = 14\,A$ and becomes $(dv_{sm}/dt)_{off} = I_0/C_r = 3.2\,V/ns$.

Note that even if a minimum off-time $t_{off} = 0$ (i.e., phase II shortened to zero) is used, the resonant transitions result in a certain voltage-time area being missing in the output voltage waveform. This limits the maximum/minimum output voltage to values that are lower/higher than $\pm V_{dc}/2$. Specifically, the maximum achievable output voltage is

$$\begin{aligned}\bar{v}_{sm,max} &= f_{sw}\int_0^{T_{sw}} v_{sm}\,d\tau \\ &= V_{dc}\left(T_{sw} - \frac{t_V}{2} - t_I - \frac{t_r}{2}\right)f_{sw} - \frac{V_{dc}}{2}.\end{aligned} \tag{7}$$

[4]Note that to account for non-ideal elements, a so-called boost current can be introduced, i.e., phase III is made slightly longer to increase the energy stored in L_r prior to the resonant transition, which compensates for losses during that transition [2]–[4]. As these are typically small, we neglect the boost current in the presented analysis.

By replacing the time intervals with their definitions from above and **Fig. 4**, we find the current-dependent maximum synthesizable output voltage amplitude $|\bar{v}_{sm,max}(I_0)|$ as

$$\frac{|\bar{v}_{sm,max}(I_0)|}{0.5V_{dc}} = \left|1 - 2\left(\frac{\pi}{2}\sqrt{L_rC_r} + \frac{2L_rI_0}{V_{dc}} + \frac{C_rV_{dc}}{2I_0}\right)f_{sw}\right|. \tag{8}$$

Note that the ARCP is also activated for turn-off transitions at low currents (see **Fig. 1(a)**) to prevent very slow switching transitions and hence very low $|\bar{v}_{sm,max}(I_0)|$. Then, the worst-case output voltage limitation occurs for the maximum output current, i.e., $I_0 = 14\,A$. As in a PV inverter application the grid voltage and the grid current are in phase (current flowing into the grid counted positive), the maximum voltage requirement occurs at the same time as the worst-case output voltage limitation. For the selected resonant circuit elements and considering $f_{sw} = 72\,kHz$, we find $\bar{v}_{sm}(I_0) \in [-336, 336]\,V$, i.e., sufficient for a grid voltage of 230 V rms. As this range narrows with increasing f_{sw}, higher switching frequencies (such as 144 kHz) are not feasible if the outlined practically relevant design criteria should be met.

A crucial aspect is to detect the turn-off condition for the main transistors, which is characterized by $i_{Lr} > i_L > 0$ (or $i_{Lr} < i_L < 0$). This can be realized with a zero-current detection (ZCD) circuit as described in [23], which should be placed at the switch-node for facilitating optimized PCB layouts. Note that the switch node is subject to dv/dt transients, but those are inherently limited to low values (less than about 3 V/ns, see above) and therefore no negative impact on the ZCD circuit's performance is expected.

2) 3L-TCM: Similarly, the detection of the TCM inductor's current zero crossing event is key for the proper operation of a 3L-TCM bridge-leg. Thus, a ZCD unit must be employed in series to the TCM inductor L_1. In contrast to an ARCP bride-leg, the switch-node potential's dv/dt is not limited and can reach high values (e.g., up to 60 V/ns). Therefore, the ZCD circuitry should be placed after the TCM inductor, i.e., on its less noisy side.

B. Semiconductor Loss Modelling and Selection

In the following, SiC MOSFETs with suitable chip areas are selected for both bridge-leg structures by considering appropriate loss models.

1) ARCP: In a first step, we consider the two main switches $T_{p,h}$ and $T_{n,l}$. As in any half-bridge operating with sinusoidal output current, they generate equal conduction losses of $P_{cond,main} = R_{ds,on}I_{out,rms}^2/2$ (per transistor). Regarding switching losses, the relatively large parallel capacitors $C_{r,p}$ and $C_{r,n}$ act as snubbers [24] and prevent any residual ZVS losses that would otherwise occur for high switched currents [14]. Thus, only C_{oss}-losses or cycle-losses [25] and gate drive losses must be considered, which are both proportional to the switching frequency. Thus, the switching losses are $P_{sw,main} = f_{sw}E_0$ (per transistor) with device-specific $E_0 = E_g + E_{cycle}$. The total semiconductor losses of the main transistors are thus $P_{main} = 2\left(P_{cond,main} + P_{sw,main}\right)$. We consider latest-generation Wolfspeed C3M 1.2 kV SiC MOSFETs in TO-247-4 packages (i.e., with a Kelvin source pin). To identify the device that results in minimum P_{main}, we select the device with the minimum available on-state resistance rating

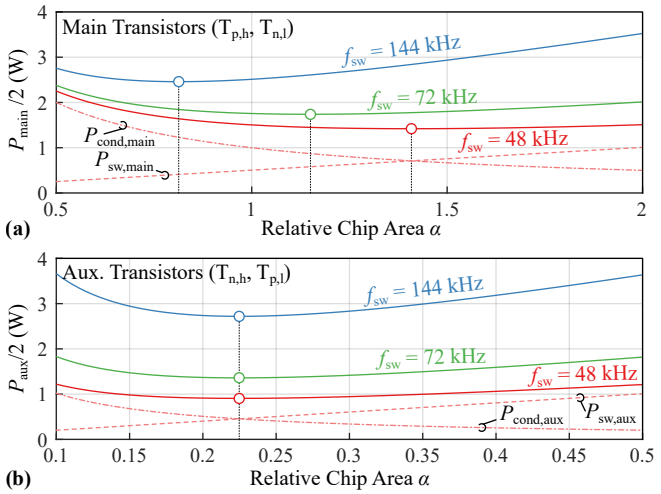

Fig. 5. Semiconductor losses of the ARCP bridge-leg's **(a)** main (see **Eq. (9)**) and **(b)** auxiliary (see **Eq. (10)**) transistors (per device) in dependence of the relative chip area α (details see text) and for the three considered f_{sw}. For f_{sw} = 48 kHz, also the conduction and switching loss components are shown.

of 16 mΩ (C3M0016120K) as a reference, which features $R'_{ds,on}$ = 20 mΩ at the design junction temperature of 100 °C and E'_0 = 10.5 µJ [14]. With α denoting the relative chip area with respect to that reference device, we find the half-bridge losses

$$P_{main}(\alpha) = I^2_{out,rms} R'_{ds,on}/\alpha + 2 f_{sw} \alpha E'_0, \tag{9}$$

as $R_{ds,on}$ scales inversely proportional with the chip area whereas E_0 increases linearly. With $dP_{main}(\alpha)/d\alpha = 0$ the relative chip area resulting in minimum total half-bridge losses (see, e.g., [26]) becomes $\alpha^2_{opt} = I^2_{out,rms} R'_{ds,on}/(2 f_{sw} E'_0)$, specifically $\alpha_{opt} = [1.40, 1.15, 0.81]$ for the considered switching frequencies $f_{sw} = [48, 72, 144]$ kHz (see **Fig. 5(a)**). Note that $\alpha > 1$ implies $R_{ds,on} < 16$ mΩ, i.e., paralleling of devices. This, however, cannot be justified for the targeted power level, and hence we select the 16 mΩ device for 48 kHz and 72 kHz; the 21 mΩ device (C3M0021120K) would be optimum for 144 kHz (although this frequency is not feasible due to control system limitations as discussed above).

In contrast to the main switches, the rms current stress of the auxiliary transistors $T_{n,h}$ and $T_{p,l}$ is frequency-dependent, as the ARCP carries out one resonant cycle per switching period, i.e., $P_{cond,aux} = f_{sw}/f_{sw,0} I^2_{Lr,rms,0} R_{ds,on}$ (per transistor), where $f_{sw,0}$ and $I_{Lr,rms,0}$ refer to a reference case. Furthermore, the auxiliary transistors are subject to zero-current but hard turn-on transitions. Thus, $Q_{oss} \cdot V_{dc}/2$ (Q_{oss} at $V_{dc}/2$) is dissipated in each switching period [27] and $P_{sw,aux} = f_{sw}/2 \cdot Q_{oss} \cdot V_{dc}/2$ (per transistor) results. Again using the relative chip area approach, we find

$$P_{aux}(\alpha) = 2 I^2_{Lr,rms,0} \frac{f_{sw}}{f_{sw,0}} \frac{R'_{ds,on}}{\alpha} + f_{sw} \alpha Q'_{oss} \frac{V_{dc}}{2} \tag{10}$$

and $\alpha^2_{opt} = 2 I^2_{Lr,rms,0} R'_{ds,on}/(f_{sw,0}\, Q'_{oss} V_{dc}/2)$. Note that the optimum relative chip area does not depend on the switching frequency. We consider again Wolfspeed's C3M series with 650 V blocking voltage rating and specifically the 15 mΩ device (C3M0015065K) as a reference with $R'_{ds,on}$ = 16.5 mΩ at the design junction temperature of 100 °C and $Q'_{oss} V_{dc}/2$ = 84 µJ. With numerical calculations for a reference case with $f_{sw,0}$ = 144 kHz, we find $I^2_{Lr,rms,0}$ = 18.5 A^2 and hence α_{opt} = 0.225. This corresponds to $R_{ds,on}$ = 67 mΩ, and thus we select the 60 mΩ device (C3M0060065K). Again, note that this device is optimum for all switching frequencies, but the loss increase at higher switching frequencies is much stronger than for the main switches (see **Fig. 5(b)**).

2) 3L-TCM: The same approach as outlined above for the ARCP brige-leg's main switches can be employed to select both, the 3L-TCM bridge-leg's 1200 V and 650 V switches, whereby we obtain the average switching frequency and the respective rms current stresses from numerical calculations. The chip-area optimization then results in $\alpha > 1$ for all considered cases, but as discussed above we do not consider paralleling of devices. Hence, we select the 16 mΩ, 1200 V (C3M0016120K) and the 15 mΩ, 650 V (C3M0015065K) devices. As in contrast to the ARCP bridge-leg, there are no snubber capacitors, and the maximum switched current is relatively high, residual ZVS losses have to be considered as described in [14]. These additional current-dependent residual ZVS losses occur only in the transistor that turns off the envelope of the (absolute) maximum current, i.e., the 1200 V devices in inverter operation. As all switching transitions occur at only half the DC-link voltage, we take the (measured) linear and quadratic loss coefficients given in [28] for 400 V. Note that these measurement results, even though taken with a symmetric half-bridge, remain valid as the effective switch-node capacitance is similar to that expected for the 3L-TCM bridge-leg.

3) Switching Cell Volume: Typically, the heat sink volume dominates the volume of a converter's semiconductor stage, and can be estimated using the cooling-system performance index (CSPI) approach proposed in [29]. However, as the per-switch losses of the considered soft-switching bridge-legs are very low (see **Fig. 5**), a heat sink-less design like used in [30] is feasible and thus considered. Then, the volume of the switching cell is mainly defined by the arrangement of the switches, the PCB layout of the gate drive circuits, and mechanical side conditions (stability, assembly), but not by the semiconductor losses. Based on similar hardware prototypes and 3D-CAD renderings, we therefore assume a fixed and identical boxed volume of 90 cm^3 for the switching cells of the ARCP and the 3L-TCM bridge-legs, which includes the switches, gate drives, commutation capacitors (and in case of the ARCP also the snubber capacitors), and a fan.

C. EMI Filter Components

The remaining volume and loss contributions required for the comparative evaluation of the two concepts come from the EMI filter inductors and capacitors. We estimate the total capacitor volume (which, in a first approximation, is equal for all considered cases as it is limited by the maximum allowable reactive power consumption) based on empirical data of a suitable commercially available foil capacitor (Panasonic ECWFG60275J). The comparably small losses in relation to the other components are neglected.

An inductor design for given specifications (inductance, low-frequency and high-frequency current stress) can make use of various degrees of freedom to adjust the inherent

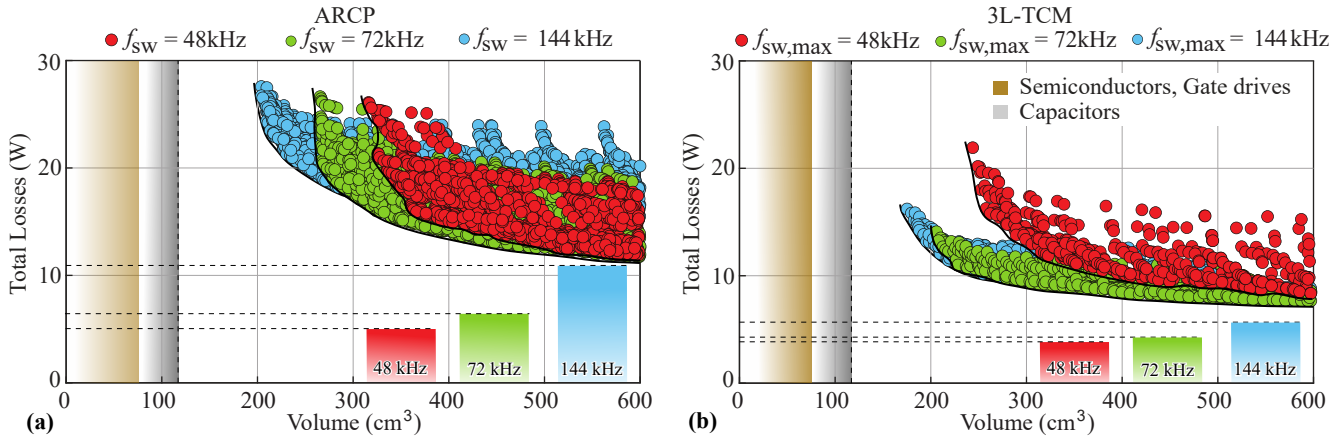

Fig. 6. Performance boundaries (loss-vs.-volume Pareto fronts) of **(a)** ARCP and **(b)** 3L-TCM inverter bridge-legs (2.2 kW, 800 V DC, CISPR 11 Class A). The Pareto fronts are obtained by combining constant volume offsets (switching stage, filter capacitors) and switching-frequency-dependent loss offsets (power semiconductors) with overall magnetics Pareto fronts; details see text. Note that ARCP designs with 144 kHz would not be feasible in practice due to duty-cycle limitations. Similarly, 3L-TCM designs with $f_{sw,max}$ = 48 kHz would be unattractive as $f_{sw,min}$ would enter the audible range.

trade-off between volume and losses, i.e., it is not sufficient to consider only a single design. Therefore, the EMI filter inductors (and the ARCP's resonant inductor) are designed with a custom Pareto optimization routine [31], considering ferrite core material, various core shapes (E, ELP, ETD, U), and different winding configurations (round solid, litz). By combining the respective Pareto-optimal designs of each component, we obtain an overall loss/volume Pareto front of the magnetic components.

IV. Comparative Evaluation

Based on the outlined design procedures for the EMI filter, chip-area-optimal (without paralleling physical devices) power semiconductors, and the passive components, **Fig. 6** shows the resulting loss-vs.-volume Pareto fronts for ARCP bridge-legs and 3L-TCM bridge-legs designed for an equal power rating and considering the same EMI regulations. We obtain the overall Pareto fronts by combining volume offsets (switching cell, filter capacitors; equal for all considered cases) and a loss offset (switching-frequency-dependent semiconductor losses) with the combined magnetics Pareto fronts discussed above.

Considering ARCP bridge-legs (see **Fig. 6(a)**), remember that f_{sw} = 144 kHz is not easily feasible in practice (timing, duty-cycle limitations) but shown for reference nevertheless. Clearly, higher switching frequencies lead to relatively high losses as a consequence of the hard-switching auxiliary transistors. This is in contrast to the fully soft-switched 3L-TCM bridge-leg (see **Fig. 6(b)**). Note that a 3L-TCM design with $f_{sw,max}$ = 48 kHz is not attractive from a loss/volume point-of-view, and also would result in undesirably low $f_{sw,min}$ = 14.9 kHz that falls within the audible range.

Fig. 7 compares the two concepts, indicating clear advantages of the 3L-TCM for the considered application—remember that the ARCP bridge-leg, even though it uses the same number of semiconductors, gate drives, etc. as the 3L-TCM bridge-leg, generates only a two-level output voltage waveform. As an example, we select designs with a total volume of 300 cm^3 (corresponding to a power density of about 7 kW/dm^3, not accounting for spacing between components, etc.): a 3L-TCM design with $f_{sw,max}$ = 72 kHz achieves total losses of about 9 W (efficiency of about 99.6 %), whereas an ARCP bridge-leg with f_{sw} = 72 kHz generates about twice as high losses (about 17 W; efficiency of about 99.2 %).

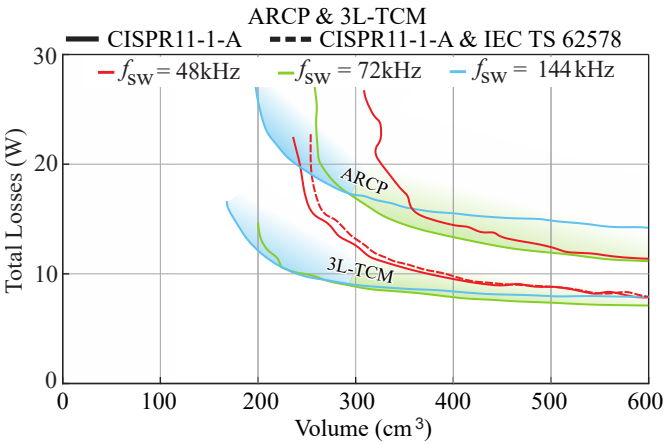

Fig. 7. Comparison of the loss-vs.-volume Pareto fronts from **Fig. 6**, and in addition those for designs that consider not only CISPR 11 Class A but also the limits for the lower frequency range of 9 kHz to 150 kHz proposed in IEC TS 62578. Note that only for the 3L-TCM design with $f_{sw,max}$ = 48 kHz a noticeable impact results.

Note further that **Fig. 7** indicates no or very little impact on the performance when considering not only CISPR 11 Class A but also upcoming EMI standards for the frequency range of 9 kHz to 150 kHz. In case of the ARCP bridge-leg, only the anyway comparably small L_2 must be slightly increased (see **Tab. II** and **Tab. III**), which does not noticeably affect the overall volume and losses. For the 3L-TCM case, we find that for f_{sw} = 144 kHz the CISPR 11 standard defines the required attenuation, whereas for f_{sw} = 72 kHz in both cases the requirement of a certain spectral separation between the CLC-filter's resonance and $f_{sw,min}$ results in sufficient attenuation to meet both standards. At f_{sw} = 48 kHz, however, the IEC TS 62578 limit requires a slightly lower cutoff frequency (i.e., a larger filter) than the spectral-separation requirement (which decides otherwise, i.e., if only CISPR 11 Class A is considered), resulting in a minor performance degradation.

V. Conclusion

As ARCP and 3L-TCM bridge-legs show a similar structure (same number of semiconductors and gate drives) and achieve soft-switching for the main (ARCP) or all (3L-TCM) power transistors, a comparative evaluation of the two approaches has been carried out considering an 800 V DC, 2.2 kW (per phase) grid-connected (i.e., subject to EMI standards) PV inverter application and switching frequencies between 48 kHz and 144 kHz. Selecting chip-area-optimal latest-generation 1200 V and 650 V SiC MOSFETs (without considering paralleling of physical devices), we find clear advantages of the 3L-TCM concept in terms of loss/volume performance, and a sweet-spot switching frequency (peak for 3L-TCM) of 72 kHz, which also prevents the minimum appearing switching frequency to fall within the audible range. In order to achieve very high power densities, 3L-TCM bridge-legs can operate with higher maximum switching frequencies (i.e., $f_{\mathrm{sw,max}} = 144\,\mathrm{kHz}$; implementations up to 150 kHz are relatively straightforward [11]). The ARCP bridge-leg's hard-switching auxiliary transistors as well as control and timing limitations (resulting in a limited output voltage range) observed in practice render the approach less suitable for high switching frequencies; and, by extension, for applications that need a full EMI filter. On the other hand, the inherent switch-node voltage dv/dt limitation is beneficial for applications with low (high-frequency) EMI noise requirements (such as aerospace, medical), or could facilitate filter-less motor drive applications. Finally, the results indicate little impact of upcoming conducted EMI limits for the frequency range of 9 kHz to 150 kHz on the resulting loss/volume Pareto fronts.

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