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Dual-Inverter Topology for Single-Phase Supplied Drive Systems without Electrolytic Capacitor

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***Abstract*—Single-phase supplied variable speed drive (VSD) systems are widely used in industrial applications and typically feature a two-stage design with a power factor corrected (PFC) boost rectifier and a three-phase voltage source inverter (VSI). However, the electrolytic DC-link capacitor, which is needed to cope with the twice grid frequency power pulsation, and the required boost inductor are unfavourable in terms of reliability, volume, cost, and complexity. Therefore, the proposed concept employs a dual-inverter topology with a three-phase open-end winding (OEW) machine, avoiding high-frequency inductors, and controls the system such that the power pulsation is buffered in the inertia of the drive train. Accordingly, the DC-link capacitance can be reduced drastically, enabling an electrolytic capacitor-less system, featuring a higher power density and an increased lifetime. This paper presents the operating principle and the corresponding closed-loop control structure, to achieve PFC operation, DC-link voltage balancing and average speed control. Detailed analysis reveals that the machine voltage can be selected independently of the grid peak voltage in contrast to existing concepts. The converter performance is evaluated based on simple performance indices with respect to the machine voltage. In the context of a 7.5 kW compressor application for railway brakes with a wide input voltage range, a semiconductor loss reduction of 30 % can be obtained compared to a state-of-the-art approach, further reducing the converter volume. Finally, the proper operation is verified with a closed-loop circuit simulation.**

***Index Terms*—Single-Phase, Electrolytic Capacitor-Less, VSD, PFC Operation, Open-End Winding PMSM, Dual-Inverter Topology**

I. Introduction

In industrial applications such as variable speed drive (VSD) systems for compressors, fans, blowers, or pumps in the lower kW range, electrical drive systems are often supplied from the single-phase AC grid in order to keep the grid interface simple [1]. Other application scenarios include higher power levels in case only a single-phase supply is available [2], i.e. in AC supplied railway systems [3], [4] or single-wire earth return (SWER) grids [5]. State-of-the-art VSD systems often employ three-phase permanent magnet synchronous machines (PMSMs) due to their high torque, low weight, high efficiency, and compactness [6]. Therefore, a power electronic system is required to convert the single-phase AC input voltage into a symmetrical three-phase voltage system with adjustable amplitude and frequency to achieve variable speed control. In addition, the system has to keep the input current proportional to the input voltage (unity power factor operation) to minimize harmonic distortion and reactive power in the grid.

Usually, all these requirements are fulfilled by a two-stage system with a single-phase power factor corrected (PFC) rectifier and a three-phase voltage source inverter (VSI), which are decoupled by an intermediate DC-link capacitor [7]. Different topologies can be employed for the PFC rectifier [8] as well as the VSI [9]. However, the most common implementation features a unidirectional single-phase boost PFC rectifier, comprising a diode bridge with a downstream boost converter and a conventional three-phase two-level VSI [10].

The inherent power pulsation of the single-phase PFC rectifier with twice the grid frequency is typically covered by a sufficiently large electrolytic DC-link capacitor with a capacitance C_{DC} in the mF-range to keep the DC-link voltage of the subsequent VSI quasi constant [11]. In summary, a state-of-the-art single-phase supplied drive system features a dedicated boost PFC rectifier input stage employing a boost inductor, a high-frequency bridge-leg and an electrolytic capacitor, which are all unfavourable in terms of reliability, volume, cost, and complexity.

Therefore, in the literature [12], [13] a vast number of single-phase supplied drive system concepts have been proposed, with the aim to avoid the boost converter and to connect the three-phase VSI directly to the diode bridge, which reduces the component count and eliminates the mentioned drawbacks. In fact, such approaches are plain simple and allow low-cost implementations, however, the input current becomes discontinuous, and PFC operation can no longer be achieved, since in the vicinity of the grid voltage zero-crossings the maximum achievable output voltage of the VSI, i.e. about half of the grid voltage amplitude, drops below the induced machine voltage, which means that the machine and input current controllability is lost. This becomes even more prominent with increasing induced machine voltage at higher rotational speeds, as it further extends the zero-current intervals and, in consequence, increases the current THD [14].

In order to regain PFC operation and complete machine current controllability, in [6] a *Single-Phase AC Dual-Inverter Topology* in combination with an open-end winding (OEW) PMSM is proposed, where a second three-phase inverter (VSI 2) employing a floating DC-link capacitor is connected to the second winding ends, while the first winding ends are attached to a first VSI (VSI 1) which is directly connected to the single-phase diode rectifier (cf. **Fig. 1(a)**). Due to

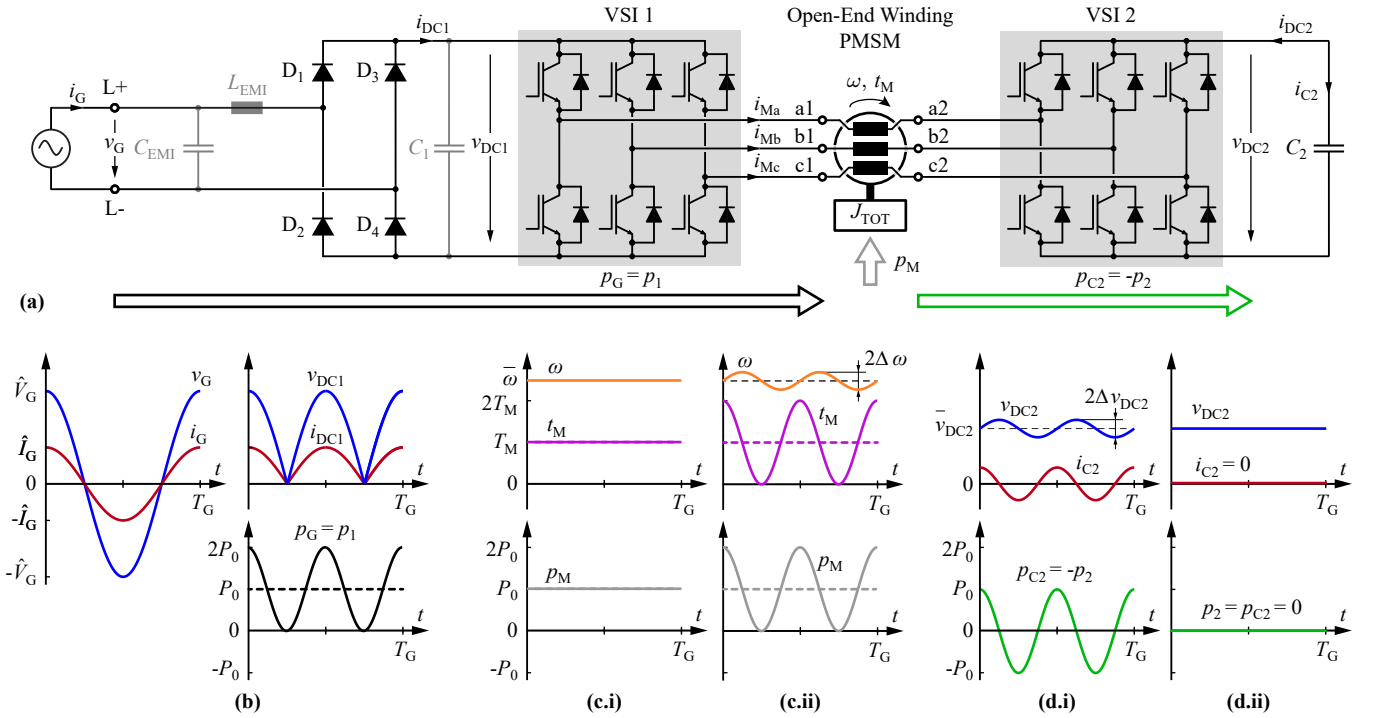

Fig. 1: **(a)** *Single-Phase AC Dual-Inverter Topology* comprising a first voltage source inverter (VSI 1) connected to the output of the diode bridge D_1-D_4, a three-phase PMSM with open-end windings, and a second voltage source inverter (VSI 2) with a floating DC-link capacitor C_2. The power flow is indicated with arrows. **(b-d)** Characteristic voltage, current, speed, torque, and power waveforms **(i)** for the state-of-the-art control scheme, where an electrolytic capacitor C_2 is required to cover the pulsating power drawn from the grid [16], [17] and **(ii)** for the proposed control scheme, where the input power pulsation is buffered by the inertia of the system, thus no electrolytic capacitor is needed.

the large machine inductances, typically in the mH-range, the switching frequency can be chosen very low, i.e. in the range of 2.5 kHz...16 kHz, and thus, both VSIs can be implemented with low-cost IGBT technology. Furthermore, the low switching frequency is not only advantageous in terms of switching losses but also for the EMI-filter requirement and the associated volume [15]. Control strategies aiming for constant rotational speed and torque operation, i.e. constant mechanical output power, are presented in [16], [17]. Related characteristic waveforms within one grid period are shown in **Fig. 1(b-d.i)**. As can be noted, since on the one hand, VSI 1 has to directly process the pulsating input power $p_\mathrm{G}(t)$ (composed of a twice grid frequency power oscillation $\tilde{p}_\mathrm{G}(t)$ with magnitude P_0 around an average input power P_0) in order to achieve PFC operation, and on the other hand, the machine is demanding a constant average output power $p_\mathrm{M}(t) = P_0$, the second inverter has to cope with the twice grid frequency zero-mean pulsating power $p_\mathrm{C2}(t) = \tilde{p}_\mathrm{G}(t)$. If active power pulsation buffer (PPB) concepts are disregarded [18], [19], this means that a large electrolytic DC-link capacitor C_DC2 for VSI 2 is required to keep v_DC2 roughly constant [17], which in turn again is a significant drawback concerning cost, volume, and especially converter lifetime [20].

In order to also eliminate the electrolytic capacitor in the *Single-Phase AC Dual-Inverter Topology*, in this paper, a novel control strategy is proposed, where the twice grid frequency power pulsation is buffered utilizing the inertia of the machine and/or drive train, which in the literature is also known as a *machine power pulsation buffer* (MPPB) [21]. As shown in **Fig. 1(b-d.ii)**, in this case, a torque t_M with a large torque ripple similar to single-phase machines is occurring for the three-phase machine, while the resulting speed ripple $\Delta\omega$ is relatively small, i.e. typically within a few percent, which is a result of the comparably large system's moment of inertia J_TOT. As a consequence, VSI 2 is only needed to apply enough voltage to the machine in order to control the machine currents, thus the active power processed by VSI 2 is zero, which means that the secondary DC-link capacitor C_2 can be small.

In order to obtain this control behaviour, however, an adaption of the operating principle and voltage division strategy for both VSIs is needed, as investigated in **Section II**. Afterwards, the control structure ensuring PFC operation in combination with DC-link voltage balancing and average speed control is derived in **Section III**. Detailed analysis reveals that in contrast to [16], [17] the machine voltage can be selected independently of the peak grid voltage, which introduces a further degree of freedom for the drive system optimization. **Section IV** illustrates this advantage for a 7.5 kW compressor application with a wide input voltage range, where the achievable system performance is evaluated and compared to the state-of-the-art. Finally, the proper closed-loop system operation is verified for the considered application by circuit simulations in **Section V**. **Section VI** summarizes the main findings of the work and gives an outlook towards future research.

II. Operating Principle and Machine Voltage Division Strategy

In the following, the operating principle and the corresponding characteristic waveforms of the *Single-Phase AC Dual-Inverter Topology* with and without electrolytic capacitor C_2 are derived in order to highlight the advantages of the proposed control strategy.

In general, in both cases, the questions arise (i) how the machine input voltage has to be divided between the two three-phase inverters VSI 1 and VSI 2, and (ii) how the machine current has to be controlled such that PFC operation is guaranteed. At the single-phase grid input, PFC operation means that the drive system has to behave as an ohmic load with a sinusoidal input current $i_\mathrm{G}(t) = \hat{I}_\mathrm{G}\cos(2\pi f_\mathrm{G} t)$ in phase with the grid voltage $v_\mathrm{G}(t) = \hat{V}_\mathrm{G}\cos(2\pi f_\mathrm{G} t)$, whereas the instantaneous input power

$$p_\mathrm{G}(t) = v_\mathrm{G}(t)\cdot i_\mathrm{G}(t) = P_0\frac{2v_\mathrm{G}^2(t)}{\hat{V}_\mathrm{G}^2} = P_0 + \tilde{p}_\mathrm{G}(t) \qquad (1)$$

is forwarded directly to the machine $p_\mathrm{M}(t)$ and/or the secondary DC-link capacitor $p_{\mathrm{C}2}(t)$. The instantaneous power balance is therefore given as

$$p_\mathrm{G}(t) = p_\mathrm{M}(t) + p_{\mathrm{C}2}(t). \qquad (2)$$

Since the secondary DC-link is floating, i.e. has no connection to the input, common-mode currents flowing through the VSIs and the machine are not possible (cf. **Fig. 1(a)**), thus the capacitor C_2 can only be charged/discharged by three-phase machine currents. Consequently, in order to simplify the system analysis, all three-phase quantities are described by their corresponding voltage and current space vectors $\underline{v}_\mathrm{M}$, $\underline{v}_1$, $\underline{v}_2$ and $\underline{i}_\mathrm{M}$ in the rotor-oriented dq-frame, i.e. $\underline{i}_\mathrm{M}(t) = i_\mathrm{Md}(t) + j i_\mathrm{Mq}(t)$, where the d-axis is aligned with the flux of the permanent magnet. In addition, an ideal non-salient pole rotor PMSM with negligible synchronous reluctance ($R_\mathrm{s} = 0$, $L_\mathrm{d} = L_\mathrm{q} \approx 0$) and a large moment of inertia J_TOT is assumed, which in all cases means that due to $L_\mathrm{d} = L_\mathrm{q} \approx 0$ (i) only the q-current component i_Mq is generating a mechanical torque, (ii) the machine terminal voltage is given by only the machine back-EMF voltage, i.e. $\underline{v}_\mathrm{M} = jV_\mathrm{P}$, and due to the large J_TOT (iii) the rotational speed ω and thus $V_\mathrm{P} = \omega p \Psi_\mathrm{PM}$ are quasi constant.

A. Dual-Inverter With Electrolytic Capacitor

Based on the power balance given in (2), there are now different possibilities to divide the pulsating input power $p_\mathrm{G}(t)$ between the machine and the secondary DC-link capacitor. However, it has to be considered that at least the average power $P_{\mathrm{C}2} = \overline{p_{\mathrm{C}2}(t)}$ of the secondary converter or the capacitor C_2 is zero. This approach is applied in the state-of-the-art concept (cf. [16]), where the machine takes a constant power equal to the average input power, i.e. $p_\mathrm{M}(t) = P_\mathrm{M} = P_0$, and the capacitor has to cope with the twice grid frequency zero-mean pulsating power, i.e. $p_{\mathrm{C}2}(t) = \tilde{p}_\mathrm{G}(t)$. Hence, due to the constant power consumption and constant back-EMF voltage of the machine, in this case, the torque $t_\mathrm{M}(t) = T_\mathrm{M}$ and

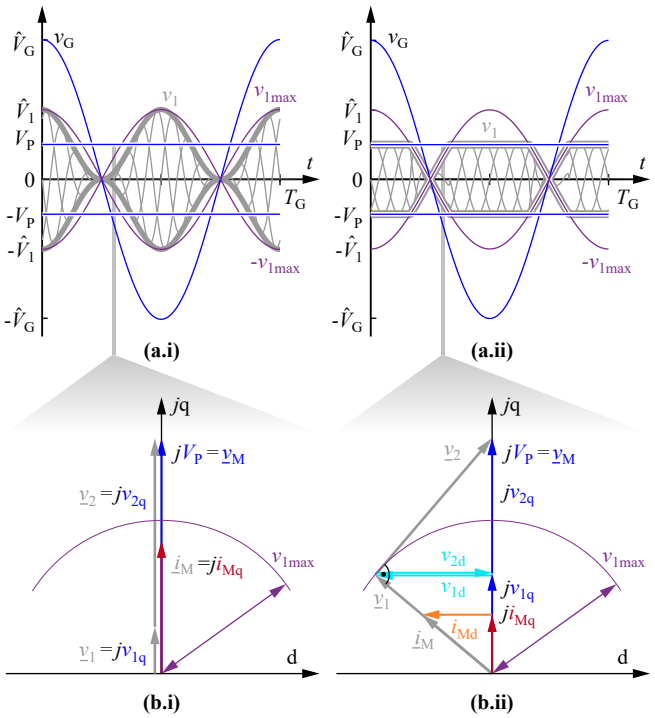

Fig. 2: (a) Voltage waveforms of the grid and the first inverter VSI 1 over one grid period T_G for **(i)** the state-of-the-art control scheme [16], [17] and for **(ii)** the proposed control scheme. **(b)** Corresponding space vector diagrams of the inverter and machine quantities in the dq-frame for $v_{1\mathrm{max}} = |v_\mathrm{G}|/2 < V_\mathrm{P}$.

thus the q-component of the machine current $i_{\mathrm{Mq}}(t)$ must also be constant. In addition, the machine current can be minimized, by selecting its magnitude equal to the q-current component, i.e. $i_\mathrm{M}(t) = i_{\mathrm{Mq}}(t) = \frac{2}{3}\frac{P_\mathrm{M}}{V_\mathrm{P}}$. The first three-phase inverter VSI 1 has to process the complete input power, i.e. $p_1(t) = p_\mathrm{G}(t)$, and as its d-voltage component is set to zero [16], i.e. $v_{1\mathrm{d}}(t) = 0$ or $v_1(t) = v_{1\mathrm{q}}(t)$, the power balance simplifies to $p_1(t) = \frac{3}{2} i_\mathrm{M}(t)\cdot v_1(t) = p_\mathrm{G}(t)$. Consequently, since $i_\mathrm{M}(t)$ is constant, the magnitude of the VSI 1 output voltage $v_1(t)$ has to vary sinusoidally with twice grid frequency as $v_1(t) = \hat{V}_1\cdot\cos^2(2\pi f_\mathrm{G} t)$ where the peak inverter voltage is limited by the maximum modulation index M_max and the peak input voltage $\hat{V}_\mathrm{G}$ as $\hat{V}_1 = M_\mathrm{max}\cdot\hat{V}_\mathrm{G}/2$ (cf. **Fig. 2(a.i)**). Due to the neglected motor inductances, the corresponding voltage space vector $\underline{v}_1(t)$ is pointing in the same direction as the motor voltage space vector $\underline{v}_\mathrm{M} = jV_\mathrm{P}$ (cf. **Fig. 2(b.i)**). Since now, the sum of the inverter voltages must correspond to the motor voltage

$$\underline{v}_\mathrm{M}(t) = \underline{v}_1(t) + \underline{v}_2(t), \qquad (3)$$

this means that in time intervals where $v_1(t)$ is smaller than V_P, the second inverter must add a voltage $\underline{v}_2(t)$ in phase with $\underline{v}_1(t)$ and $\underline{i}_\mathrm{M}(t)$, i.e. VSI 2 delivers power from the secondary DC-link capacitor C_2 to the machine, whereas in time intervals where $v_1(t)$ is larger than V_P, the second inverter must add a voltage $\underline{v}_2(t)$ out of phase by 180° with respect to $\underline{v}_1(t)$ and $\underline{i}_\mathrm{M}$, i.e. VSI 2 delivers power from the machine to the secondary DC-link capacitor. Hence, in order to ensure that the average power $P_{\mathrm{C}2}$ within one grid half-period is zero,

the machine voltage V_P must be equal to $\hat{V}_1/2$, which for a maximum modulation index $M_\mathrm{max} = 1$ results in a maximum machine voltage of $V_\mathrm{P} = \hat{V}_\mathrm{G}/4$. In this case, the maximum voltage amplitude of VSI 2 is required at the grid voltage zero-crossing, where it has to provide the full machine voltage V_P, thus the length of the voltage vector of VSI 2 varies between $-V_\mathrm{P}$ and V_P, which requires a secondary DC-link of $V_\mathrm{DC2} > 2V_\mathrm{P}$. Furthermore, since the zero-mean pulsating input power is covered by the secondary DC-link capacitor, a large capacitance C_2 is needed to keep the voltage fluctuation within certain limits, which in [17] is given as

$$C_2 > \frac{2P_0}{2\pi f_\mathrm{G}\left(v_\mathrm{DC2,max}^2 - v_\mathrm{DC2,min}^2\right)}. \tag{4}$$

All corresponding characteristic waveforms of this control concept are shown in **Fig. 4(a)**.

B. Dual-Inverter Without Electrolytic Capacitor

Instead of keeping only the average power P_C2 at zero, it is also possible to keep the instantaneous power directly at zero, i.e. $p_\mathrm{C2}(t) = 0$. This means that the secondary converter is only needed to control the machine current and the complete pulsating input power is delivered directly to the machine, i.e. $p_\mathrm{M}(t) = p_\mathrm{G}(t)$. Since due to the large J_TOT it is assumed that the rotational speed ω and thus the motor voltage amplitude V_P are still constant, the q-component of the machine current now has to vary sinusoidally with twice grid frequency,

$$i_\mathrm{Mq}(t) = \frac{2}{3}\frac{p_\mathrm{M}(t)}{V_\mathrm{P}} = \hat{I}_\mathrm{M} \cdot \cos^2\left(2\pi f_\mathrm{G} t\right), \tag{5}$$

with $\hat{I}_\mathrm{M} = 4/3\ P_0/V_\mathrm{P}$, which clearly results in a proportional mechanical torque $t_\mathrm{M}(t)$ (cf. **Fig. 1(c.ii)**). In contrast to the previously described concept, the voltage space vector of the secondary inverter $\underline{v}_2(t)$ must now be either zero or perpendicular to the machine current $\underline{i}_\mathrm{M}(t)$ in order to guarantee that $p_\mathrm{C2}(t) = p_2(t) = 0$. Considering (3), this means that $i_\mathrm{M}(t) = i_\mathrm{Mq}(t)$ is only possible in time intervals where $v_\mathrm{1max}(t) = |v_\mathrm{G}(t)|/2 \geq V_\mathrm{P}$, and thus $\underline{v}_1(t)$ and $\underline{v}_2(t)$ can be selected to $\underline{v}_1(t) = jV_\mathrm{P}$ (cf. **Fig. 2(a.ii)**) and $\underline{v}_2(t) = 0$, respectively. In time intervals where $v_\mathrm{1max}(t) < V_\mathrm{P}$, however, an additional negative d-current component $i_\mathrm{Md}(t)$ must be flowing through the machine, such that $\underline{v}_2(t)$ can be kept perpendicular to the machine current $\underline{i}_\mathrm{M}(t)$ (cf. **Fig. 2(b.ii)**). In contrast, $\underline{v}_1(t)$ is advantageously chosen in phase with $\underline{i}_\mathrm{M}(t)$ and its magnitude is equal to $v_\mathrm{1max}(t)$, i.e. $v_1(t) = v_\mathrm{1max}(t)$ or $M_1 = 1$, such that the rms currents in both inverters and the machine are minimized. Hence, from the power balance at VSI 1, i.e. $p_1(t) = \frac{3}{2}\underline{v}_1(t) \cdot \underline{i}_\mathrm{M}(t) = \frac{3}{2}v_1(t) \cdot i_\mathrm{M}(t) = p_\mathrm{G}(t)$, the total machine current $i_\mathrm{M}(t)$ can be calculated as

$$i_\mathrm{M}(t) = \frac{2}{3}\frac{p_\mathrm{G}(t)}{v_1(t)}, \tag{6}$$

and in combination with the given q-current component $i_\mathrm{Mq}(t)$ also the d-current $i_\mathrm{Md}(t)$ can be deduced as

$$i_\mathrm{Md}(t) = -\sqrt{i_\mathrm{M}^2(t) - i_\mathrm{Mq}^2(t)}. \tag{7}$$

Furthermore, since $\underline{v}_1(t)$ and $\underline{i}_\mathrm{M}(t)$ are selected to be in phase and $v_1(t) = v_\mathrm{1max}(t)$, the d- and q-voltage components $v_\mathrm{1d}(t)$ and $v_\mathrm{1q}(t)$ of VSI 1 are proportional to the d- and q-current components $i_\mathrm{Md}(t)$ and $i_\mathrm{Mq}(t)$ of the motor, which results in

$$v_\mathrm{1d}(t) = i_\mathrm{Md}(t)\frac{v_1(t)}{i_\mathrm{M}(t)} \quad \text{and} \quad v_\mathrm{1q}(t) = i_\mathrm{Mq}(t)\frac{v_1(t)}{i_\mathrm{M}(t)}. \tag{8}$$

Finally, the remaining d- and q-voltage components $v_\mathrm{2d}(t)$ and $v_\mathrm{2q}(t)$ of the secondary inverter need to fulfil (3) and are found as

$$v_\mathrm{2d}(t) = -v_\mathrm{1d}(t) \quad \text{and} \quad v_\mathrm{2q}(t) = V_\mathrm{P} - v_\mathrm{1q}(t). \tag{9}$$

The corresponding characteristic waveforms of the proposed control concept are shown in **Fig. 4(b)** and **(c)**. It has to be mentioned that in this case the machine voltage V_P is no longer limited by the input voltage $v_\mathrm{G}(t)$, since the secondary DC-link voltage V_DC2 can be selected arbitrarily high - clearly limited by e.g. the blocking voltage capability of the used semiconductor switches. However, as will be shown in **Section IV**, this offers a further degree of freedom in the design of the single-phase supplied drive system.

III. Control Structure

In the following, the closed-loop control structure to ensure the proposed operating behaviour of the single-phase supplied dual-inverter drive system is described in detail. Basically, the drive system must operate the machine at the desired average speed, while on the one hand, PFC operation must be guaranteed at the input, and on the other hand, the DC-link voltage of the secondary inverter must be regulated to a certain target voltage. In principle, this can be done in analogy to a conventional cascaded motor control with a slow outer *Speed Control* block and a fast inner *Machine Current Control* block, whereby the two mentioned conditions must be taken into account (cf. **Fig. 3**). In particular, the motor control has to be extended by (i) the additional *DC-Link Voltage Control* block, which demands a certain power p_C2^* to charge/discharge the secondary DC-link capacitor C_2 and together with the required input power p_G^* determines the instantaneous power consumption p_M^* and current i_Mq^* of the machine, and by (ii) the *Machine Voltage Division* block, which divides the machine voltage between the two three-phase inverters in such a way that only the second inverter is used for the motor current control while the first inverter adjusts its voltage to guarantee PFC operation. This means that the input current i_G is only defined by the impressed machine current i_M and the selected modulation index of VSI 1, which is in contrast to two-stage drive systems with dedicated boost PFC rectifiers, where an additional closed-loop grid current control is implemented [10], [21]. The individual control blocks of the proposed structure shown in **Fig. 3** are explained in the following.

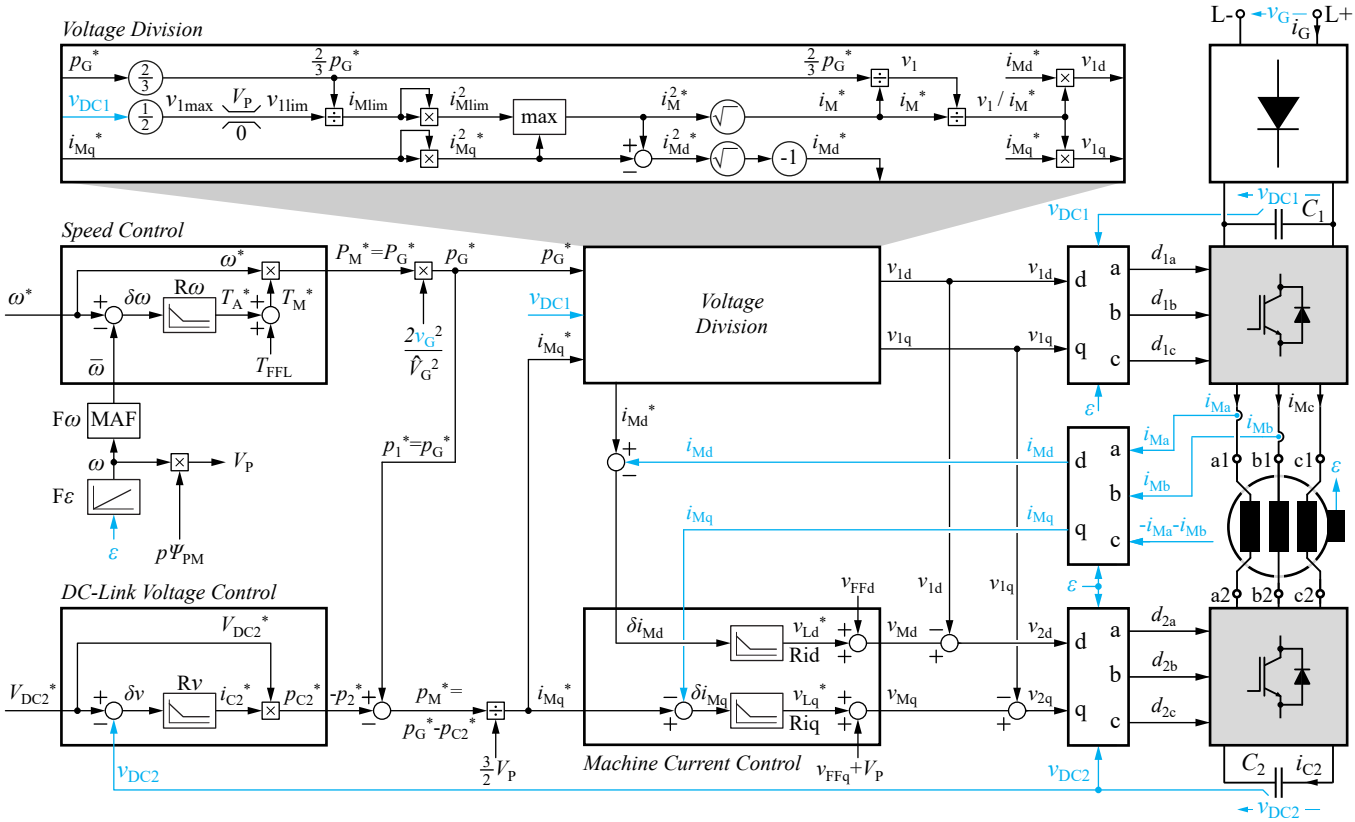

Fig. 3: Proposed control structure of the electrolytic capacitor-less *Single-Phase AC Dual-Inverter Topology*, consisting of four main blocks, i.e. *Speed Control*, *DC-Link Voltage Control*, *Voltage Division*, and *Machine Current Control*, to achieve average speed control, PFC operation, and voltage balancing at the secondary DC-link. Measurement quantities are shown in blue, indicating that only two current sensors are required to reduce costs.

A. Speed Control

Starting with the outermost control loop, the *Speed Control* block provides at its output the required average machine power P_{M}^* to reach the commanded rotational speed ω^*. At the input, the reference speed ω^* is compared with the average mechanical speed $\bar{\omega}$ calculated from the measured mechanical angle ε, which is also used for the dq-transformation [22]. As a consequence of the described power/torque pulsation, the actual mechanical speed ω, which is also used to calculate the amplitude of induced motor voltage V_{P}, features a certain ripple with twice grid frequency $2f_{\mathrm{G}}$. Hence, a moving average filter (MAF) [23] with a time constant of $T_{\mathrm{G}}/2$ is needed to obtain the average speed $\bar{\omega}$. The speed controller Rω then uses the calculated speed error $\delta\omega$ to determine the required torque T_{A}^*, which together with the optional feed-forward load torque T_{FFL} gives the reference torque T_{M}^* and from this the required machine power P_{M}^*. Assuming a lossless system, P_{M}^* equals the average input power P_{G}^*, which based on (1) leads together with the measured input voltage v_{G} to the commanded instantaneous input power p_{G}^*.

B. DC-Link Voltage Control

The amount of instantaneous power p_{M}^* that is actually delivered to the machine also depends on how much power p_{C2}^* has to be delivered/consumed by the secondary inverter to charge/discharge the capacitor C_2, which is determined by the *DC-Link Voltage Control* block.

The reference voltage of the secondary DC-link V_{DC2}^* can be set according to the actual system's operating point, but must always be larger than $2V_{\mathrm{P}}$ (cf. **Section II**). The DC-link voltage controller Rv then compares V_{DC2}^* with the measured voltage v_{DC2} and translates the voltage error δv into the required capacitance current i_{C2}^*, which together with V_{DC2}^* results in the required power demand p_{C2}^* to bring the DC-link voltage back to its reference value. The instantaneous machine power $p_{\mathrm{M}}^* = p_{\mathrm{G}}^* - p_{\mathrm{C2}}^*$ is then used to calculate the reference of the machine's q-current component i_{Mq}^* (cf. (5)), which is finally forwarded to the two inner blocks.

C. Voltage Division

The reference values p_{G}^* and i_{Mq}^* commanded from the outer control loops are now processed in the inner *Voltage Division* block to calculate on the one hand, the d-current reference value i_{Md}^* needed for the *Motor Current Control* block, and on the other hand, the d- and q-voltages of the first inverter to guarantee PFC operation.

As described in **Section II**, i_{Md}^* can directly be calculated from (6) and (7), however, for i_{M}^* it has to be considered that the maximum achievable inverter voltage v_1 is given by the actual input voltage to $v_{1\mathrm{max}} = |v_{\mathrm{G}}|/2 = v_{\mathrm{DC1}}/2$ and in addition is limited to the machine voltage V_{P} if $v_{1\mathrm{max}} > V_{\mathrm{P}}$.

In special cases where (6) results in a motor current amplitude i^*_{M} which is smaller than the commanded q-component i^*_{Mq}, i^*_{M} has to be increased to i^*_{Mq} such that (7) leads to a feasible d-current. Consequently, in order to still comply with the commanded input power p^*_{G}, the voltage v_1 of the first inverter has to be reduced. In the *Voltage Division* block this is implemented by recalculating v_1 from the commanded machine current i^*_{M} by using (6) again. Subsequently, the individual voltage components $v_{1\mathrm{d}}$ and $v_{1\mathrm{q}}$ are calculated from v_1 based on (8).

D. Machine Current Control

Since now the two reference machine currents i^*_{Md} and i^*_{Mq} are known, the *Machine Current Control* block can be implemented in the same way as in the conventional cascaded machine control. There, the current controllers Rid and Riq translate the current errors δi_{Md} and δi_{Mq} into the reference inductor voltages v^*_{Ld} and v^*_{Lq}. In addition, the machine voltages due to cross-couplings between d- and q-axis as well as the induced speed voltages can be added as feed-forward terms, i.e. $v_{\mathrm{FFd}} = -\omega p L_{\mathrm{q}} i^*_{\mathrm{Mq}}$ and $v_{\mathrm{FFq}} = \omega p L_{\mathrm{d}} i^*_{\mathrm{Md}} + V_{\mathrm{P}}$, which leads to the required machine voltages v_{Md} and v_{Mq}. Finally, the already derived voltage components of VSI 1 $v_{1\mathrm{d}}$ and $v_{1\mathrm{q}}$ are subtracted to obtain the remaining voltages of the secondary inverter $v_{2\mathrm{d}}$ and $v_{2\mathrm{q}}$.

IV. Comparative Evaluation

The performance of the proposed electrolytic capacitor-less solution is evaluated in the context of a $7.5\,\mathrm{kW}$ single-phase supplied compressor system for railway brakes with the specifications given in **Tab. I**. The system is supplied from the tertiary transformer winding of the railway vehicle, which in nominal operation provides a single-phase rms voltage of $400\,\mathrm{V}/50\,\mathrm{Hz}$, however, due to large voltage tolerances of the railway grid, can vary in a wide range between $360\,\mathrm{V}$ and $480\,\mathrm{V}$.

Based on these specifications, in the following the influence of the proposed control strategy on the system design is compared with the state-of-the-art, i.e. the occurring voltage and current stresses, and characteristic waveforms are analyzed and compared.

A. Dual-Inverter With Electrolytic Capacitor

As given in [16] and also deduced in **Section II**, for the state-of-the-art system the maximum acceptable machine voltage is limited to $V_{\mathrm{P}} = \hat{V}_{\mathrm{G}}/4$, which for the minimum grid voltage results in $V_{\mathrm{P}} = 127\,\mathrm{V}$. Hence, a machine with a maximum machine constant of $k_{\mathrm{V}} = p\,\Psi_{\mathrm{PM}} = V_{\mathrm{P}}/\omega = 0.33\,\mathrm{Vs}$ can be selected, and for a maximum input power of $9\,\mathrm{kW}$ a machine peak current of $i_{\mathrm{Mq}} = I_0 = 47\,\mathrm{A}$, i.e. a machine phase rms current of $I_{\mathrm{PH0rms}} = I_0/\sqrt{2} = 33\,\mathrm{A}$, results. The corresponding waveforms are shown in **Fig. 4(a)**.

B. Dual-Inverter Without Electrolytic Capacitor

Assuming a machine with the same machine constant of $k_{\mathrm{V}} = 0.33\,\mathrm{Vs}$, the current stresses for the proposed control concept can directly be calculated, and result in a pulsating q-current with an average current of $I_0 = 47\,\mathrm{A}$ and a comparably small d-current component such that the phase current can be approximated by $I_{\mathrm{PHrms}} = \sqrt{3/2} I_{\mathrm{PH0rms}} = 41\,\mathrm{A}$ [21]. Thus, the elimination of the electrolytic capacitor comes at the expense of increased conduction losses and a poor utilization of VSI 2, which for the same machine voltage $V_{\mathrm{P}} = V_0 = \hat{V}_{\mathrm{Gmin}}/4$ is actually only needed in close vicinity of the grid voltage zero-crossings (cf. **Fig. 4(b)**). Consequently, for the proposed control concept a machine with a larger machine constant k_{V} should be selected, since no limitation by the grid voltage exists, and a higher machine voltage decreases the average q-current (cf. (5)) and extends the operating interval of VSI 2. As shown in **Fig. 4(c)**, for example, doubling the machine voltage to $V_{\mathrm{P}} = 2V_0 = \hat{V}_{\mathrm{Gmin}}/2$ leads to a continuous operation of both VSIs and reduces the machine phase current to $I_{\mathrm{PHrms}} = 24\,\mathrm{A}$, which is below the phase current obtained with the state-of-the-art system, even though the d-current is increased now. Clearly, it has to be mentioned that the voltage stresses at the semiconductor devices of VSI 2 and the secondary DC-link capacitor C_2 are now increasing.

In **Fig. 5(a)**, the dependency of the phase current and DC-link voltage stresses with respect to the selected machine voltage are illustrated for a range of $V_{\mathrm{P}} \in [V_0, 3V_0] = [127\,\mathrm{V}, 382\,\mathrm{V}]$. It can be noticed that for low machine voltages the q-current scales inversely proportional to the machine voltage, i.e. $I_{\mathrm{PHqrms}} = 1/\sqrt{3}\; P_0/V_{\mathrm{P}}$, and thus also the machine phase current I_{PHrms} reduces similarly. However, as soon as the machine voltage V_{P} exceeds $\hat{V}_{\mathrm{G}}/2$, the first inverter is operated continuously with $M = 1$ and i_{M} becomes proportional to $|i_{\mathrm{G}}|$ (cf. (6)). Thus, for a given input power this means that i_{M} remains unchanged even if the machine voltage is further increased. As shown in **Fig. 5(a)**, this transition point clearly depends on the actual grid rms voltage and for the minimum grid voltage actually also represents the optimum design point. This can be verified by using simple performance indices to estimate the dependency of conduction and switching losses of both VSIs on the selected machine voltage [24].

The conduction losses of inverters employing IGBTs with antiparallel diodes, depend on the average and rms currents flowing through the devices. Assuming similar conduction behaviour for the IGBT and the antiparallel diode, the overall semiconductor conduction losses, can be assessed by the sum

TABLE I: Summary of the system specifications.

Description	Parameter	Nominal Value
Nominal Mechanical Power	$P_{\mathrm{M,N}}$	$7.5\,\mathrm{kW}$
Nominal Mechanical Speed	n_{N}	$3700\,\mathrm{rpm}$
Grid Power	P_{G}	$9\,\mathrm{kW}$
Grid Voltage	V_{Grms}	$360...480\,\mathrm{V}$
Grid Frequency	f_{G}	$50\,\mathrm{Hz}$
Switching Frequency	f_{SW}	$16\,\mathrm{kHz}$

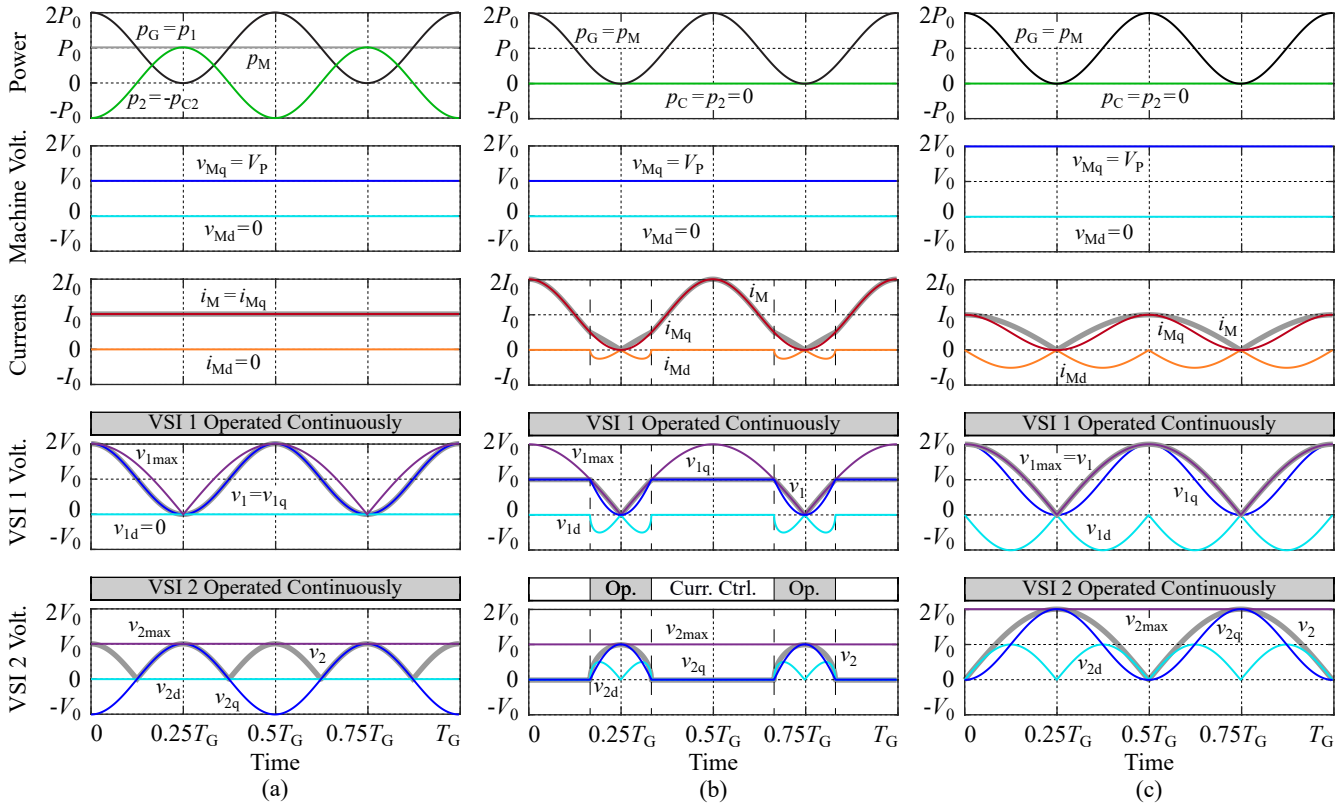

Fig. 4: Characteristic waveforms over one grid period T_G for **(a)** the state-of-the-art control scheme with an electrolytic capacitor for the maximum machine voltage $V_\mathrm{P} = V_0 = \hat{V}_\mathrm{G}/4$, **(b)** the proposed solution for $V_\mathrm{P} = V_0 = \hat{V}_\mathrm{G}/4$ causing increased machine currents and **(c)** the proposed solution for $V_\mathrm{P} = 2V_0 = \hat{V}_\mathrm{G}/2$, achieving a reduced machine current stress compared to (a).

of the average currents and the sum of the squared rms currents

$$\rho_\mathrm{avg} = \sum_k \left(I_{\mathrm{Davg},k} + I_{\mathrm{Tavg},k}\right) \tag{10}$$

$$\rho_\mathrm{rms} = \sum_k \left(I^2_{\mathrm{Drms},k} + I^2_{\mathrm{Trms},k}\right). \tag{11}$$

Furthermore, assuming a linear dependency of the semiconductor switching losses on both the switched voltage v_T and the switched current i_T, the overall switching losses can be assessed by the sum of the product $v_\mathrm{T} i_\mathrm{T}$ averaged over one grid period T_G as

$$\varsigma = \sum_k \langle v_{\mathrm{T},k}\ i_{\mathrm{T},k} \rangle_{T_\mathrm{G}}. \tag{12}$$

Fig. 5(b) shows the dependency of the introduced performance indices ρ_avg, ρ_rms, and ς scaled to the corresponding values of the state-of-the-art system, i.e. $\rho_{0\mathrm{avg}} = 180\,\mathrm{A}$, $\rho_{0\mathrm{rms}} = 6.7\,\mathrm{kA}^2$ and $\varsigma_0 = 62\,\mathrm{kVA}$, with respect to the selected machine voltage. For a given input voltage it clearly turns out that $\rho_\mathrm{avg}/\rho_{0\mathrm{avg}}$ and $\rho_\mathrm{rms}/\rho_{0\mathrm{rms}}$ decrease with increasing machine voltage as long as $V_\mathrm{P} \leq \hat{V}_\mathrm{G}/2$ and afterwards stay constant. On the other hand, ς/ς_0 also decreases until $V_\mathrm{P} = \hat{V}_\mathrm{G}/2$, however, afterwards increases again due to the increasing switched voltage v_T. Consequently, in terms of inverter losses, the optimum machine voltage is found at the transition point $V_\mathrm{P} = 2V_0 = \hat{V}_{\mathrm{Gmin}}/2$, where compared to the state-of-the-art system roughly $45\,\%$ lower conduction losses and around $15\,\%$ lower switching losses are achieved.

Assuming an inverter design with equal conduction and switching losses, an overall loss reduction of around $30\,\%$ can be obtained, which besides the elimination of the electrolytic capacitor also reflect in a substantially smaller heatsink volume.

V. System Verification

In a first step, the proper operation of the electrolytic capacitor-less drive system implementing the proposed closed-loop control structure of **Section III** is verified by circuit simulations. The simulation is conducted for the nominal operating point of the underlying application with an output power of $7.5\,\mathrm{kW}$ at $3700\,\mathrm{rpm}$ and an input supply voltage of $400\,\mathrm{V}/50\,\mathrm{Hz}$. As deduced in **Section IV**, the performance optimum of the converter is achieved at $V_\mathrm{P} = 2V_0 = 255\,\mathrm{V}$, resulting in a machine constant of $k_{\mathrm{Vopt}} = 0.66\,\mathrm{Vs}$. Hence, the PMSM 1FT7084 from Siemens [25], characterized by $k_\mathrm{V} = 0.65\,\mathrm{Vs}$, is employed. The moment of inertia of the drive train is assumed to be $J_\mathrm{TOT} = 13.5\,\mathrm{mkgm}^2$. The machine parameters and selected circuit parameters are summarized in **Tab. II**.

The simulated steady-state waveforms for $V_\mathrm{Grms} = 400\,\mathrm{V}$ and $V_\mathrm{P} \approx 250\,\mathrm{V}$ are shown in **Fig. 6**. The instantaneous voltage ratio $v_{1\mathrm{max}}/V_\mathrm{P}$ defines the envelope of the machine

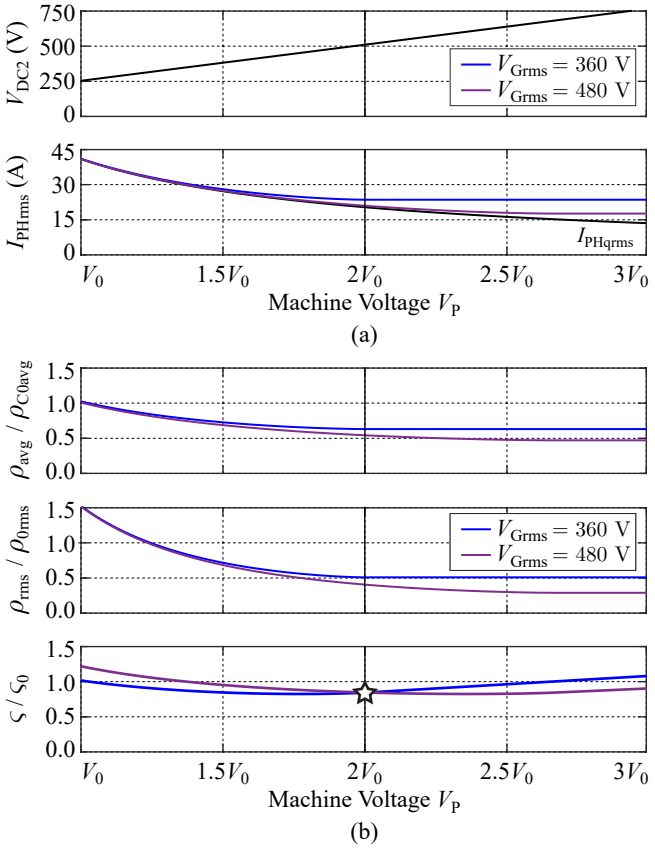

Fig. 5: Performance evaluation of the proposed electrolytic capacitor-less dual-inverter concept with respect to the machine voltage $V_P = V_0 ... 3V_0$; **(a)** Secondary DC-link voltage V_{DC2} and phase current stress I_{PHrms} for the minimum and maximum grid voltage. **(b)** Loss related performance indices scaled to the corresponding values of the state-of-the-art system, indicating a significant improvement for all indices at the selected machine voltage $V_P = 2V_0 = 255\,\mathrm{V}$.

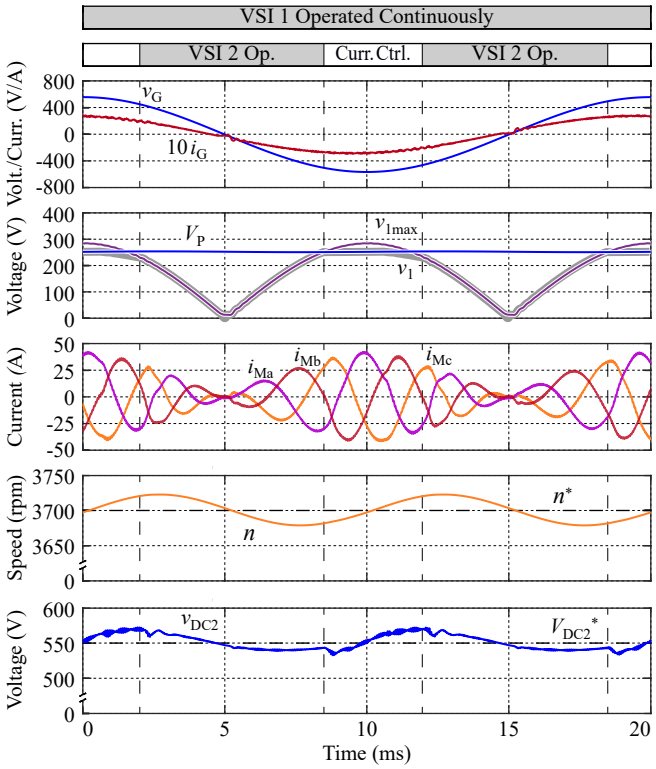

Fig. 6: Simulated steady-state waveforms for the proposed electrolytic capacitor-less single-phase AC dual-inverter concept showing the grid, dual-inverter, machine and DC-link waveforms as well as the operating mode within one grid period $T_G = 20\,\mathrm{ms}$. The corresponding references are indicated by dashed lines.

TABLE II: Summary of the machine and circuit parameters.

Description	Parameter	Nominal Value
Voltage Constant	k_V	0.65 Vs
Number of Pole Pairs	p	5
Machine Inductance	$L_d = L_q$	2.8 mH
Machine Inertia	J_M	4.5 mkgm^2
Drive Train Inertia	J_{TOT}	13.5 mkgm^2
EMI Capacitor	C_{EMI}	10 µF
EMI Inductor	L_{EMI}	70 µH
Input Capacitor	C_1	10 µF
DC-Link Capacitor	C_2	50 µF

phase currents i_{Ma}, i_{Mb} and i_{Mc}, which contains a fundamental component with $2f_G = 100\,\mathrm{Hz}$, as well as the required operation mode. As can be noted, since v_{1max} is exceeding V_P, there are time intervals where either both VSIs have to actively apply a voltage to the machine or where VSI 2 is only used to control the machine current, i.e. $v_1 < v_{1max}$ or $M_1 < 1$. It can be noticed that the resulting interval for $M_1 < 1$ is slightly extended compared to $v_{1max} > V_P$, which is a direct consequence of the non-zero reference capacitor power $p^*_{C2} \neq 0$. Regardless of this, the control keeps the grid current i_G sinusoidal and in phase with the grid voltage v_G, verifying PFC operation. The achieved THD is below 4 % and is mainly limited by the passive diode bridge, which causes current distortions in the vicinity of the voltage zero-crossings.

Furthermore, the speed controller ensures an average speed $\bar{\omega}$ equal to the reference, whereas the actual speed shows a ripple of $\Delta\omega = P_0 / (4\pi f_G \bar{\omega} J_{TOT}) = 2.3\,\mathrm{rad/sec}$, i.e. 22 rpm or around 0.6 % [21]. The DC-link reference voltage is set to $V^*_{DC2} = 550\,\mathrm{V}$, which is above $2V_P \approx 500\,\mathrm{V}$ to ensure full controllability even during voltage deviations. Theoretically, the secondary DC-link voltage would be constant, however, a limited controller bandwidth and disturbances are causing a certain voltage fluctuation of around 35 V. In a conventional system, this voltage ripple would correspond to a DC-link capacitance of 1.2 mF, which is 24 times larger than the capacitance used in the proposed solution without electrolytic capacitors.

VI. Conclusions

In this paper, a novel control strategy for the single-phase AC dual-inverter topology is proposed, where twice grid frequency power pulsation is covered by the inertia of the drive train, such that no electrolytic DC-link capacitor is required. The corresponding operating principle, including the machine voltage division strategy and the machine current reference

generation, and the introduced control structure, which ensures a sinusoidal input current, the requested average speed, and a certain DC-link voltage, are explained in detail. The proper operation is verified by circuit simulations, achieving a DC-link voltage ripple of $35\,\mathrm{V}$ in a $7.5\,\mathrm{kW}$ system with a DC-link capacitance of only $50\,\mu\mathrm{F}$. In contrast to the state-of-the-art, the analyzed concept does not feature an inherent grid-voltage dependent limit on the maximum achievable machine voltage. Thus, the system performance is evaluated with respect to this additional degree of freedom. Simple performance indices assess the corresponding converter losses, and the loss minimum is achieved for a machine voltage equal to half the peak grid voltage. For the analyzed compressor application with a wide input voltage range, the semiconductor losses can be reduced by 30 % compared to the state-of-the-art dual-inverter system with electrolytic capacitor.

Hence, the proposed concept overcomes the limitations of a conventional operation of the single-phase AC dual-inverter topology and therefore is a promising solution to substantially improve the converter system's power density and avoid electrolytic capacitors, also increasing the converter's lifetime.

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