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Vienna Rectifier Front-End Dual Three-Phase PMSM Drive with Synergetic Control

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***Abstract*—This paper proposes a novel Vienna rectifier-based dual three-phase permanent magnet synchronous machine (VR-dPMSM) drive system. In contrast to conventional solutions relying on two independent two-level rectifiers, the proposed topology uses a single Vienna rectifier (VR) to supply two stacked inverters driving a dual three-phase machine. This architecture enables the exclusive use of 600 V semiconductor devices, allowing for implementations with either SiC or GaN technology. The partitioned DC link reduces capacitance requirements, enabling the use of film or ceramic capacitors. A synergetic control strategy between the VR and the stacked inverters is introduced, enabling a *1/3-PWM* modulation mode that reduces switching losses in the VR by up to two-thirds. In addition, the VR can adjust the DC link voltages based on machine speed, which can help to minimize the switching losses in the stacked inverters. A cascaded control structure is analyzed to coordinate power factor correction, midpoint current regulation in the VR, and motor control. Time-domain simulations of a 25 kW system confirm sinusoidal grid currents, VR-dPMSM speed control, and reduced switching activity in the VR in *1/3-PWM* and *2/3-PWM* modes, validating the operation of the proposed VR-dPMSM drive concept and its synergetic control.**

***Index Terms*—Vienna Rectifier, Dual Three-Phase Machine, Multiphase Drives, Synergetic Control, 1/3 PWM, Modular Inverter Architecture, Electric Drive Systems**

I. Introduction

Grid-connected drive systems typically consist of a PWM rectifier that supplies an intermediate DC-link voltage, which in turn powers an inverter driving the motor [1]. The grid voltage, for example 3Φ $400\,\mathrm{V_{rms}}$, is rectified and regulated by the front-end rectifier to a typical DC-link voltage of $800\,\mathrm{V_{dc}}$. From this DC link, the inverter generates controlled motor currents to produce the required torque for the mechanical load. In such drive systems, the power semiconductors used in both the rectifier and the inverter withstand blocking voltages must be rated for $1.2\,\mathrm{kV}$.

Compared to widely used three-phase machines, multiphase machines with more than three phases offer improved fault tolerance and enable the distribution of motor power and current across a larger number of phases [2], thereby reducing the current stress on each phase and switching device.

Among them, six-phase machines are frequently considered, as they can be derived from conventional and widely available three-phase machines through relatively simple modifications, such as splitting the phase belt into two halves, resulting in a so-called dual three-phase machine [3]. A dual three-phase machine features two electrically isolated three-phase winding systems on the stator and thus requires two three-phase inverters for independent control of phase currents. These inverters can either be supplied from the same rectifier in a parallel configuration, as shown in [4], [5], or from two separate rectifiers, as demonstrated in [6]. However, such converter arrangements tend to be bulky and complex, and they still require $1.2\,\mathrm{kV}$ rated power semiconductors.

In this paper, we propose a novel drive system topology in which a Vienna rectifier (VR) supplies two inverters that drive a dual three-phase machine, as illustrated in **Fig. 1**. To the best of our knowledge, this topology has not been reported in the literature before. The VR ensures power factor correction (PFC) operation and offers several advantages over conventional two-level rectifiers, including reduced volume of input inductors ($L_\mathrm{a}, L_\mathrm{b}, L_\mathrm{c}$) and the ability to generate a symmetrically partitioned DC link voltage. This structure allows for the direct connection of two inverters, each controlling one of the electrically isolated three-phase winding systems of the dual three-phase machine. In this work, we specifically focus on a permanent magnet synchronous machine (PMSM) implementation of the dual three-phase machine, as shown in **Fig. 1**.

The proposed Vienna rectifier-based dual three-phase PMSM (VR-dPMSM) drive system offers an advantage in terms of semiconductor technology, enabling the use of $600\,\mathrm{V}$ devices. This allows the entire system to be implemented with $600\,\mathrm{V}$ SiC MOSFETs, as shown in **Fig. 1(a)**, or alternatively with $600\,\mathrm{V}$ GaN devices, as illustrated in **Fig. 1(b)**. The latter results in a fully GaN-based VR-dPMSM drive system, which is an important feature, as it enables the use of modern GaN semiconductor devices, such as the GaN monolithic bidirectional switch (MBDS) [7], in the VR front-end stage. Beyond the technical advantages, this is also highly beneficial from a sustainability perspective: the CO_2 footprint to manufacture and ship GaN devices is up to ten times lower than that of silicon, and the end-application footprint can be reduced by up to $30\,\%$ [8].

A further advantage of the proposed VR-dPMSM concept is the possibility to reduce the required DC link capacitance compared to two-level systems, enabling the exclusive use of

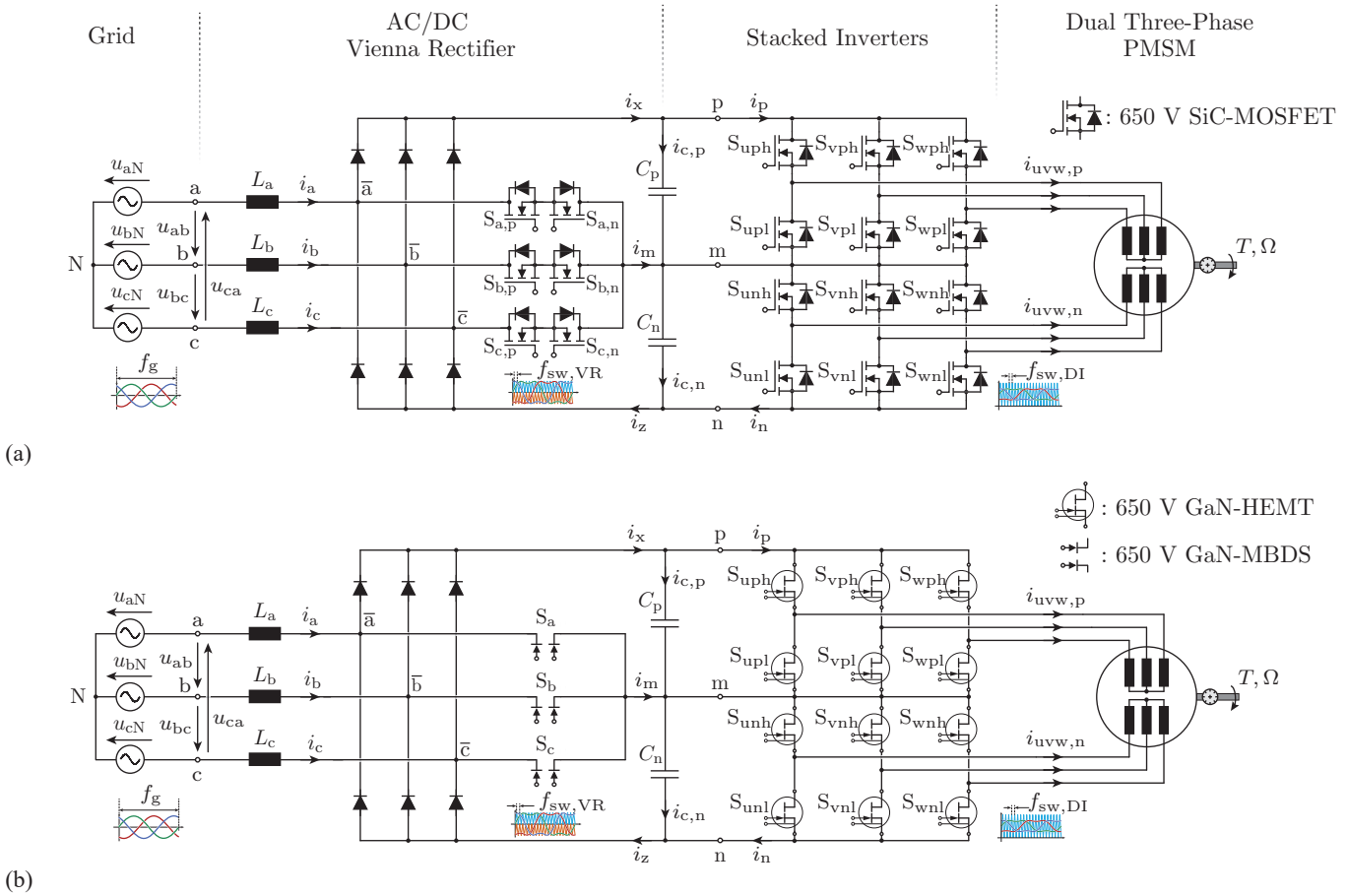

Fig. 1: Circuit diagram of the proposed Vienna rectifier-based dual three-phase PMSM (VR-dPMSM) drive system. **(a)** Implementation using 600 V SiC semiconductor technology. **(b)** Implementation using 600 V GaN semiconductor technology. Note: diodes need to be 1.2 kV.

film or ceramic capacitor technology. A similar approach was demonstrated in [9], where film capacitors were employed in the DC link of a drive system featuring a three-level T-type rectifier and a three-level T-type inverter supplying an induction machine. Additionally, the stacked inverter structure often benefits in terms of electromagnetic interference (EMI) mitigation. For instance, EMI noise generated by the stacked VSIs can be reduced by phase-shifting the carrier signals of the upper and lower inverters [10].

In terms of control, the proposed VR-dPMSM concept offers several advantages. Since the VR operates as a boost-type converter, it allows for flexible adjustment of the cascaded DC link voltages u_{pm} and u_{mn} depending on the operating conditions. At higher motor speeds, these voltages can be increased to ensure that the stacked inverters are capable of maintaining proper current control in the presence of elevated back-EMF levels. Conversely, at lower speeds, the voltages can be reduced to minimize switching losses. Additionally, at lower DC link voltages, the VR can operate in the so-called *1/3 modulation* mode, where high-frequency PWM is applied only during one third of the fundamental period, specifically, during the interval when the grid current is minimal and crossing zero [11]. This modulation strategy requires the inverters to actively regulate the DC link voltages such that their total follows the line-to-line grid voltage waveform. We refer to this coordinated operation between the VR and the inverters as *synergetic control* of the VR-dPMSM system, which will be explained in detail in the following sections.

This paper is organized as follows: **Section II** discusses the operating principle of the VR-dPMSM drive system, and **Section III** describes the corresponding control structure. **Section IV** presents simulation results for a 25 kW VR-dPMSM drive system, followed by the conclusion in **Section V**.

II. Operation Principle of the dPMSM

The proposed VR-dPMSM drive system is illustrated in **Fig. 1**, featuring implementations with either SiC or fully GaN-based semiconductor technology. The power stage of the system is configured by combining a VR as the front-end stage with stacked inverters as the back-end stage. This arrangement naturally interfaces with the three-point output of the VR and the two sets of three-phase windings of the dual three-phase PMSM. This section explains how the VR and the stacked inverters can be controlled either non-synergistic or in a synergetic manner, depending on the speed of the dual three-phase PMSM, aiming to minimize overall switching losses in

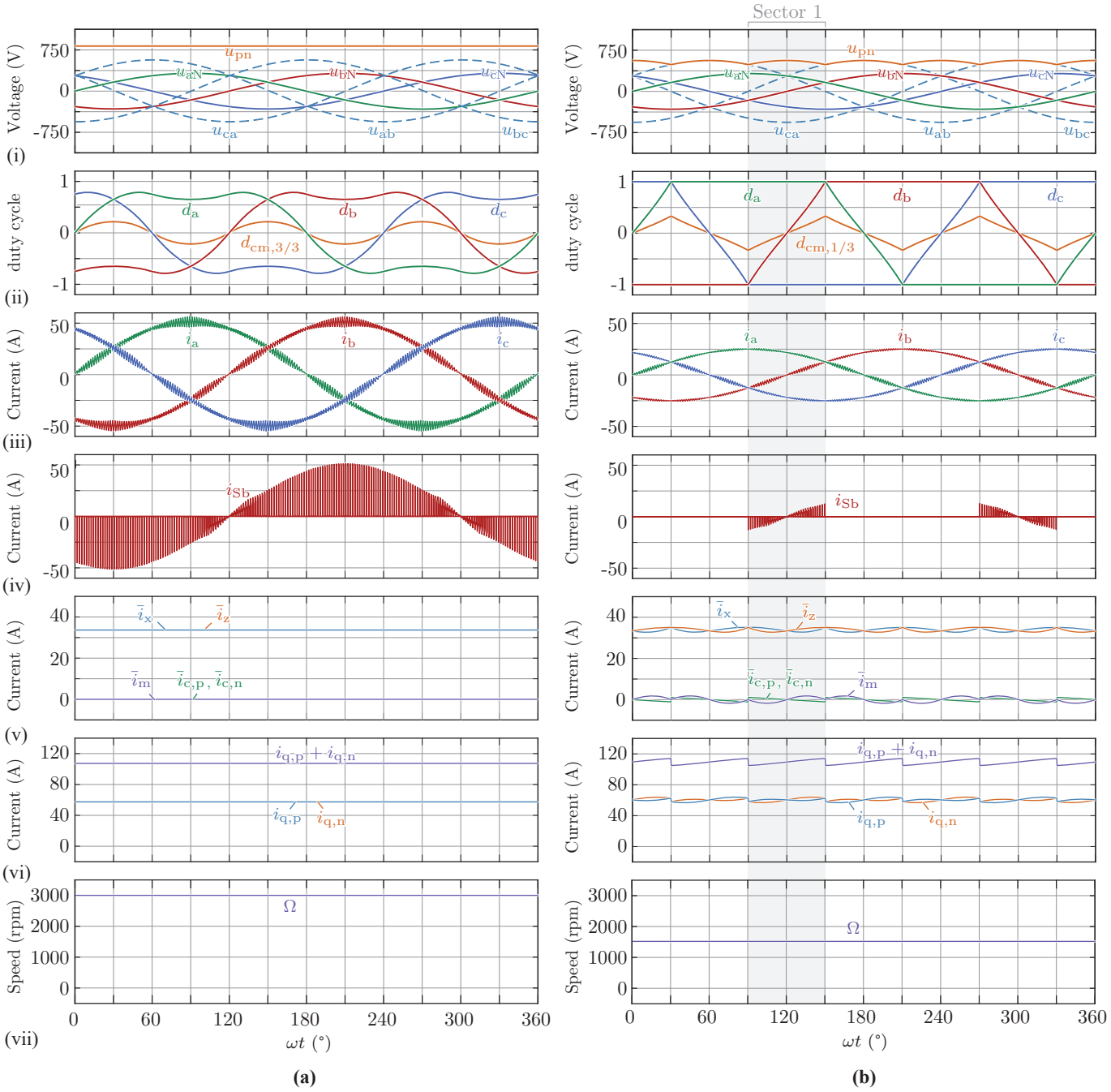

Fig. 2: Characteristic waveforms for **(a)** high-speed operation with fully boosted DC-link voltage by VR of 3/3-PWM mode at 25 kW, **(b)** low-speed operation with partially DC-link current controlled by stacked inverters at 12.5 kW. From top to bottom: (i) input grid voltages u_{iN} for $i = \{a, b, c\}$ along with the DC-link voltage u_{pn}, (ii) phase-leg duty cycles d_i and common mode duty cycle d_{cm} of VR (where $d_i = 1$ denotes that the high-side diode of VR is clamping the corresponding phase-leg to the positive DC-link rail p, and $d_i = -1$ denotes that the low-side diode is clamping the phase-leg to the corresponding phase-leg to the negative DC-link rail n), (iii) mains phase current i_i, (iv) current through the bi-directional switch S_b, (v) local averaged currents through the DC-link of VR $\{\bar{i}_x, \bar{i}_z\}$, mid-point current of VR $\bar{i}_m$, and DC-link capacitor current $\bar{i}_C$, (vi) q-axis current $i_{q,p}$ and $i_{q,n}$ of the stacked inverters connected to the corresponding DC-link rails, (vii) rotational speed of the dual three-phase PMSM. For illustrative purposes, the waveforms are calculated for a low switching frequency of 10 kHz and input inductances of 2 mH, and a constant load torque of 79.6 N m is assumed for both speeds.

the drive by reducing the switching action and keeping the DC link voltages as low as possible.

For dPMSM operation at high speeds, the elevated back-EMF requires the stacked inverters to operate with increased DC link voltages in order to maintain control over the phase currents. Since the VR functions as a boost-type converter, it can regulate the DC link voltages u_{pm} and u_{mn} to the required level. However, the maximum allowable voltage is limited by the blocking capability of the semiconductors used in both the VR and the stacked inverters. For example, when using $600\,\mathrm{V}$ rated devices, each of the DC link voltages u_{pm} and u_{mn} should not exceed $400\,\mathrm{V}$.

The key waveforms corresponding to high-speed operation at $3000\,\mathrm{rpm}$ and an output power of $25\,\mathrm{kW}$ are shown in **Fig. 2(a)**. In this scenario, the total DC link voltage $u_{\mathrm{pn}} = u_{\mathrm{pm}} + u_{\mathrm{mn}}$ must be boosted, e.g., to $760\,\mathrm{V}$, to provide sufficient voltage headroom for the stacked inverters. This ensures that adequate voltage margin is available for current control in the presence of elevated back-EMF (see (8)), as illustrated in **Fig. 2(a.i)**. Under these conditions, the VR operates as a boost-type power factor correction (PFC) rectifier, while the stacked inverters regulate the dPMSM phase currents according to a field-oriented control (FOC) strategy to deliver the required torque at the machine shaft. In this high-speed scenario where VR is boosting the DC link voltages, the DC link capacitors serve to decouple the rectifier and inverter stages, allowing both to operate in a conventional and a non-synergistic manner.

This operating mode, in which the VR boosts the DC link voltage, is referred to as *3/3-PWM* mode. In this mode, all three bidirectional switches $\mathrm{S_a}$, $\mathrm{S_b}$, and $\mathrm{S_c}$ are actively pulse-width modulated throughout the entire mains period, as illustrated in **Fig. 2(a.ii)**. It is well established in the literature [12] that, under such operating conditions, achieving a zero midpoint current i_{m} requires the application of a specific common-mode voltage:

$$u_{\mathrm{cm,3/3}} = u_{\mathrm{mid}} \left(1 - \frac{|u_{\mathrm{mid}}|}{\max(|u_{\mathrm{min}}|, |u_{\mathrm{max}}|)}\right), \qquad (1)$$

where $u_{\mathrm{min}}, u_{\mathrm{mid}}$ and u_{max} are defined after sorting the VR switching node voltages $\{\bar{u}_{\bar{\mathrm{a}}}, \bar{u}_{\bar{\mathrm{b}}}, \bar{u}_{\bar{\mathrm{c}}}\}$[1] such that $u_{\mathrm{max}} > u_{\mathrm{mid}} > u_{\mathrm{min}}$. This, in turn, leads to a corresponding common-mode duty cycle component $d_{\mathrm{cm,3/3}}$, as also shown in **Fig. 2(a.ii)**.

As a result of the PFC operation, the grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ remain sinusoidal, and the current through the bidirectional switches follows the envelope of these grid currents, as illustrated in **Fig. 2(a.iii,a.iv)**. During steady-state operation of the dPMSM under constant power conditions, the local average values over the switching period of the DC link currents $\bar{i}_{\mathrm{x}}$ and $\bar{i}_{\mathrm{z}}$ are constant. At the same time, the local average values of the midpoint current and the capacitor currents are zero, i.e., $\bar{i}_{\mathrm{m}} = 0$ and $\bar{i}_{\mathrm{c,p}} = \bar{i}_{\mathrm{c,n}} = 0$, as shown in **Fig. 2(a.v)**.

[1]The overbar denotes the local average over the switching period, e.g., $\bar{u}_{\bar{\mathrm{a}}}$ is the averaged value over the switching period of $u_{\bar{\mathrm{a}}}$.

As mentioned, $\bar{i}_{\mathrm{m}} = 0$ is achieved through the VR's midpoint current regulation strategy [12] by adding the common-mode voltage (1) to the voltage references of nodes $\bar{\mathrm{a}}$, $\bar{\mathrm{b}}$, $\bar{\mathrm{c}}$, obtained by the grid current controller, which ensures that the power P_{VR} is equally transferred to the two DC links of the stacked inverters.

The total power is then delivered to the machine and converted into mechanical output by the stacked inverters, which regulate the q-axis currents $i_{\mathrm{q,p}}$ and $i_{\mathrm{q,n}}$, as depicted in **Fig. 2(a.vi)**. This results in continuous mechanical rotation of the dPMSM, as shown in **Fig. 2(a.vii)**.

When the speed of the dPMSM decreases, the required DC link voltages u_{pm} and u_{mn} can be reduced to minimize switching losses. However, the total DC link voltage $u_{\mathrm{pn}} = u_{\mathrm{pm}} + u_{\mathrm{mn}}$ cannot fall below the line-to-line grid voltage. For example, in **Fig. 2(b)**, during operation in *Sector 1*, the diode in phase a is clamped to the positive rail p, while the diode in phase c is clamped to the negative rail n. The question now arises how the input grid currents are maintained sinusoidal. Due to the three-wire grid connection of the PFC VR stage, it is sufficient to independently control only two of the three input currents, e.g., i_{a} and i_{c}, as illustrated in *Sector 1* of **Fig. 2(b)**. The third current i_{b} is then determined by Kirchhoff's Current Law (KCL): $i_{\mathrm{b}} = -(i_{\mathrm{a}} + i_{\mathrm{c}})$.

To control two input currents, two degrees of freedom are required. These are provided by the ability to generate two of the line-to-line voltages in the VR stage, namely, $u_{\overline{\mathrm{ab}}}$ and $u_{\overline{\mathrm{bc}}}$. Together with the given mains voltages (u_{ab} and u_{bc}) and the KCL constraint, these voltages determine the instantaneous voltages across the input inductors L_{a}, L_{b}, and L_{c}, which ultimately shape the input currents.

As explained in detail in [11], controlling only the DC link voltages would result in current flow through only the most positive and most negative grid phases, with equal magnitude and opposite direction. Consequently, the current in the middle phase, for example, phase b in *Sector 1*, would be zero, and a proper sinusoidal set of three-phase currents would not be established.

To ensure sinusoidal and balanced three-phase currents that are in phase with the grid voltages, an additional current must be impressed in the middle phase. This current is proportional to the middle phase voltage in each voltage sector. As shown in **Fig. 2(b.iv)**, the middle phase current always equals the minimum absolute value among the three phase currents. It is symmetric around zero and exhibits a quasi-triangular waveform under PFC operation, being positive for 30° and negative for the subsequent 30° within each 60° wide voltage sector.

Depending on the active voltage sector, this middle-phase current can be impressed by pulse-width modulating the bidirectional switch corresponding to the middle phase. For instance, in *Sector 1*, the middle phase is phase b, and thus the switch $\mathrm{S_b}$ is modulated accordingly.

For the complete VR-dPMSM drive system, this operating principle implies that the stacked inverters must regulate the voltages across the DC-link capacitors during the clamping

intervals. In other words, within each voltage sector, two of the three phase currents are directly regulated at a time, one by the VR and the other by one of the stacked inverters, while the specifically controlled phases alternate every 30° sub-interval according to the active voltage vector.

For example, during the first 30° of Sector 1, the upper-side inverter directly controls i_{a}, whereas the VR regulates i_{b}. The remaining phase current, i_{c}, is then determined by KCL. During the subsequent 30°, the lower-side inverter directly controls i_{c}, while the VR continues to regulate i_{b}; consequently, i_{a} is determined by KCL.

This coordinated operation between the VR and the stacked inverters is referred to as *synergetic control*. The corresponding modulation mode is known as *1/3-PWM* mode [11], [13], as the VR performs high-frequency PWM switching only during one third of the grid period. This reduces switching losses in the VR stage by a factor of $2/3$.

During *1/3-PWM* operation of the VR, an additional current component is superimposed onto the quadrature motor currents to facilitate power exchange between the DC link capacitors (C_{p} and C_{n}) and the mechanical inertia of the drive train. This is necessary to maintain the desired voltage profiles u_{pm} and u_{mn}, i.e. to shape the total DC link voltage u_{pn} according to the maximum line-to-line grid voltage, as shown in **Fig. 2(b.i)**. To achieve this voltage waveform across the capacitors, the averaged capacitor currents $\bar{i}_{\mathrm{c,p}}$ and $\bar{i}_{\mathrm{c,n}}$ follow a piecewise linear profile, illustrated in **Fig. 2(b.v)**. This behavior causes the quadrature motor currents $i_{\mathrm{q,p}}$ and $i_{\mathrm{q,n}}$ to oscillate accordingly, as seen in **Fig. 2(b.vi)**. The computation of these quadrature current references is explained in detail in the following section, which addresses the control strategy of the VR-dPMSM drive system. Due to the high inertia of the drive train, these quadrature current oscillations that correspond to torque oscillations of the dPMSM, have a negligible impact on the mechanical speed, which remains essentially constant throughout the operation, as shown in **Fig. 2(b.vii)**.

Similar to the *3/3-PWM* mode, the *1/3-PWM* mode of the VR also requires a common-mode voltage to be added to the phase voltage reference. The expression for this common-mode voltage is given [14] as

$$u_{\mathrm{cm},1/3} = u_{\mathrm{cm},1/3,\mathrm{max}} = u_{\mathrm{cm},1/3,\mathrm{min}}, \tag{2}$$

where

$$\begin{aligned} u_{\mathrm{cm},1/3,\mathrm{max}} &= \frac{u_{\mathrm{pn}}}{2} - u_{\mathrm{max}}, \\ u_{\mathrm{cm},1/3,\mathrm{min}} &= -\frac{u_{\mathrm{pn}}}{2} - u_{\mathrm{min}}. \end{aligned} \tag{3}$$

During transitions between the *3/3-PWM* and *1/3-PWM* modes, or in intermediate operating conditions, the system enters the so-called *2/3-PWM* mode. In this mode, the common-mode voltage switches between the expressions defined for the *3/3-PWM* mode (1) and the *1/3-PWM* mode (2). The common-mode voltage with the smaller absolute value is always selected, ensuring minimal switching loss and compliance with voltage limits [14]. Thus, the resulting general expression for the common-mode voltage, valid for any VR PWM mode, is given as

$$u_{\mathrm{cm}} = \max\left(u_{\mathrm{cm},1/3,\mathrm{min}},\, \min(u_{\mathrm{cm},1/3,\mathrm{max}},\, u_{\mathrm{cm},3/3})\right). \tag{4}$$

The total DC link voltage u_{pn} is calculated based on the common-mode voltages of each operating mode. The detailed derivation is provided in the Appendix.

III. Control Structure of the VR-dPMSM

The control structure of the VR-dPMSM drive system is illustrated in **Fig. 3**. The control scheme ensures proper operation of the drive in accordance with the principles discussed in **Sec. II**, including seamless transitions between the different PWM modes–*1/3*, *2/3*, and *3/3*.

The VR-dPMSM control structure shown in **Fig. 3** follows a cascaded architecture. The outermost and slowest loop is the speed controller, which is followed by the DC link voltage controller operating with approximately five times higher bandwidth. The innermost loops are the grid current and motor current controllers, each designed with a bandwidth roughly five times higher than that of the voltage controller.

In the speed control loop, shown in **Fig. 3(b.i)**, the desired dPMSM speed reference Ω^* is compared with the measured speed Ω to compute the speed error. This error is processed by a PI-type feedback controller, which generates the required torque reference T^* to ensure that the dPMSM follows the speed command. The mechanical power reference for the VR input stage is then computed as the product of the speed and torque references, i.e., $P^*_{\mathrm{VR}} = \Omega^*\, T^*$. As shown in the control scheme in **Fig. 3(b)**, this power reference is passed to the VR current control and the DC link voltage control blocks.

A conventional approach for controlling the VR input grid currents to ensure power factor correction (PFC) is to compute a reference conductance G^* from the VR power reference and the measured grid voltage amplitude as $G^* = P^*_{\mathrm{VR}}/(\frac{3}{2}\hat{U}_{\mathrm{ac}})$. Multiplying G^* with the instantaneous measured grid phase voltages yields the current references i^*_{a}, i^*_{b}, and i^*_{c}. These references are then compared with the measured grid currents, and the resulting errors are processed by P (or PI) controller to generate the required voltage references across the grid inductors: u^*_{La}, u^*_{Lb}, and u^*_{Lc}. The switching-node voltage references are obtained by subtracting these inductor voltage references from the measured grid phase voltages:

$$u^*_{\bar{\mathrm{a}}} = u_{\mathrm{a}} - u^*_{\mathrm{La}}, \quad u^*_{\bar{\mathrm{b}}} = u_{\mathrm{b}} - u^*_{\mathrm{Lb}}, \quad u^*_{\bar{\mathrm{c}}} = u_{\mathrm{c}} - u^*_{\mathrm{Lc}},$$

as shown in **Fig. 3(b.ii)**. Based on these switching-node references, the common-mode voltage u^*_{cm} and the DC link voltage reference u^*_{pn} are computed as described in **Sec. II** and forwarded to the VR modulator and subsequent control stages.

The voltage controller block, shown in **Fig. 3(b.iii)**, ensures proper regulation of the DC link voltages u_{pm} and u_{mn}, which is essential for selecting the correct PWM operating mode (see **Sec. II**). The total DC link voltage reference u^*_{pn} is computed according to (5), and the individual DC link voltage references are then set as $u^*_{\mathrm{pm}} = u^*_{\mathrm{mn}} = u^*_{\mathrm{pn}}/2$. PI controllers are

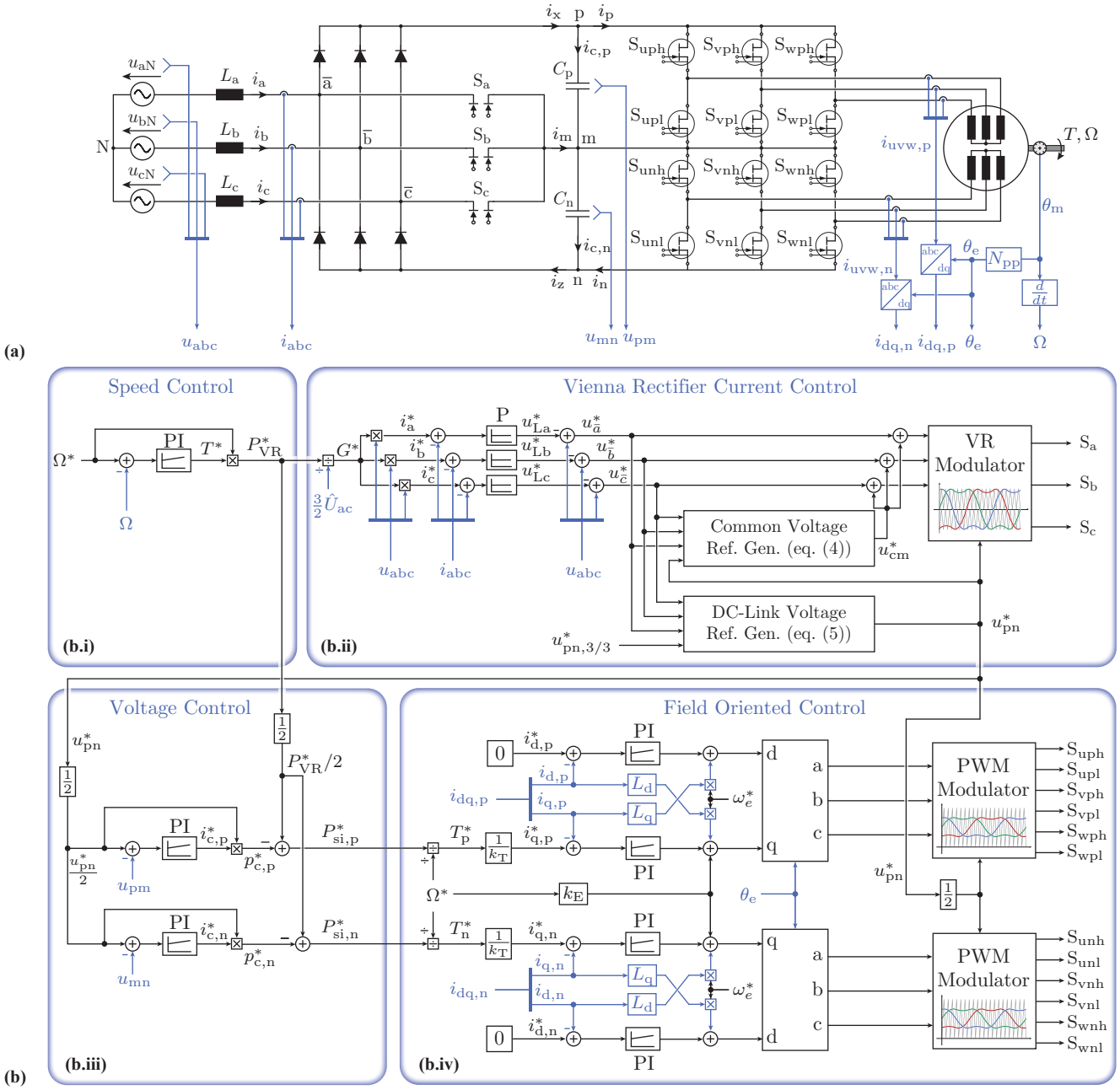

Fig. 3: Control structure of the VR-dPMSM drive system: **(a)** schematic with measurement points (parameters indicated in blue); **(b)** control diagram comprising **(b.i)** speed control, **(b.ii)** grid-current control with common-mode voltage and DC-link voltage reference generator (cf. [14]), **(b.iii)** voltage control for the DC-link capacitors, and **(b.iv)** field-oriented control (FOC).

used to regulate these voltages by calculating the required capacitor currents $i^*_{\mathrm{c,p}}$ and $i^*_{\mathrm{c,n}}$, which are then multiplied by their respective voltage references to obtain the capacitor power demands, $p^*_{\mathrm{c,p}}$ and $p^*_{\mathrm{c,n}}$. These capacitor power demands are subtracted from the available VR output power per inverter leg, i.e., $P^*_{\mathrm{VR}}/2$, to yield the resulting power references for the stacked inverters, $P^*_{\mathrm{si,p}}$ and $P^*_{\mathrm{si,n}}$, i.e., the dPMSM. Since the VR provides the total power, e.g., for the upper DC link, $P^*_{\mathrm{VR}}/2 = p^*_{\mathrm{c,p}} + p^*_{\mathrm{si,p}}$, the capacitor power must be subtracted to obtain the actual motor power. It should be noted that, under ideal steady-state conditions, during steady-state operation in the *3/3-PWM* mode, the capacitor voltages remain constant, and therefore the corresponding power references are zero: $p^*_{\mathrm{c,p}} = p^*_{\mathrm{c,n}} = 0$.

From the stacked inverter power references $P^*_{\mathrm{si,p}}$ and $P^*_{\mathrm{si,n}}$, the torque references for the two winding sets of the dPMSM are calculated as $T^*_{\mathrm{p}} = \frac{P^*_{\mathrm{si,p}}}{\Omega}$ and $T^*_{\mathrm{n}} = \frac{P^*_{\mathrm{si,n}}}{\Omega}$. These torque references are then used to compute the quadrature current components by dividing each torque reference by the torque constant k_{T}. The resulting current references are used within the field-oriented control (FOC) framework to regulate the dPMSM, ultimately producing the gate signals for the stacked

TABLE I: Simulation parameters.

Parameter	Symbol	Value
Vienna Rectifier		
Grid voltage (line to neutral)	$\hat{U}_{\mathrm{ac}}$	$325\,\mathrm{Vpk}$
Grid frequency	f_{g}	$50\,\mathrm{Hz}$
Switching frequency	$f_{\mathrm{sw,vr}}$	$100\,\mathrm{kHz}$
Input inductance	$L_{\{\mathrm{a,b,c}\}}$	$100\,\mu\mathrm{H}$
DC-link voltage	u_{pn}	$560\,\mathrm{V}$ to $800\,\mathrm{V}$
DC-link capacitance	$C_{\mathrm{p}}, C_{\mathrm{n}}$	$10\,\mu\mathrm{F}$
Stacked Inverters		
DC-link voltage	$u_{\mathrm{pm}}, u_{\mathrm{mn}}$	$280\,\mathrm{V}$ to $500\,\mathrm{V}$
Switching frequency	$f_{\mathrm{sw,si}}$	$100\,\mathrm{kHz}$
dPMSM		
Flux linkage	$\hat{\Phi}$	$0.25\,\mathrm{Wb}$
Stator inductance	L_{s}	$2\,\mathrm{mH}$
Number of pole pairs	N_{pp}	2
Moment of inertia	J	$0.0446\,\mathrm{kg\,m^2}$
Nominal phase voltage peak	$\hat{U}$	$260\,\mathrm{V}$
Nominal load torque	$T_{\mathrm{load,nom}}$	$79.6\,\mathrm{Nm}$
Nominal mech. power	P_{nom}	$25\,\mathrm{kW}$
Nominal mech. speed	n_{nom}	$3000\,\mathrm{rpm}$
Control Parameters		
Bandwidth of speed controller	$f_{\mathrm{bw,speed}}$	$400\,\mathrm{Hz}$
Bandwidth of VR current controller	$f_{\mathrm{bw,vr}}$	$10\,\mathrm{kHz}$
Bandwidth of voltage controller	$f_{\mathrm{bw,voltage}}$	$2\,\mathrm{kHz}$
Bandwidth of dq current controller	$f_{\mathrm{bw,dq}}$	$10\,\mathrm{kHz}$

inverters.

IV. Simulation Results

To validate the operation of the proposed VR-dPMSM drive system, a time-domain simulation was performed using the schematic and control structure shown in **Fig. 3**. The numerical parameters used in the simulation are summarized in **Tab. I**.

To demonstrate the successful operation of the VR-dPMSM drive across all three PWM modes, 1/3, 2/3, and 3/3, a time-domain simulation was conducted in which the system starts at half the nominal speed ($1500\,\mathrm{rpm}$) and accelerates to the nominal speed ($3000\,\mathrm{rpm}$) using a linear speed reference ramp over a period of $0.5\,\mathrm{s}$ while being loaded with the torque linearly proportional to the speed $T_{\mathrm{load}} = k_{\mathrm{fric}}\Omega$, where the friction coefficient is $k_{\mathrm{fric}} = 0.158\,\mathrm{Nms}$, at which nominal mechanical power of $25\,\mathrm{kW}$ is developed for nominal mechanical speed of $3000\,\mathrm{rpm}$. At the beginning of the acceleration, when the speed is low, the VR-dPMSM operates in *1/3-PWM* mode. As the machine reaches nominal speed, the system transitions into the *3/3-PWM* mode, as shown in **Fig. 4**.

At the initial operating point, during *1/3-PWM* mode, the DC link voltage is regulated to follow the grid line-to-line voltage. This requires shaping the total DC link voltage u_{pn} to form an envelope that tracks the peak line-to-line grid voltage. As explained in **Sec. III**, this is achieved by regulating the power of the stacked inverters accordingly, which introduces an oscillating component in the quadrature current references, as shown in **Fig. 4(b.vi)**. In simple terms, this oscillating power component causes a periodic exchange of energy between the DC link capacitors and the mechanical inertia of the dPMSM drive train, enabling the required voltage shaping, enabling the *1/3-PWM* mode on the VR.

As the speed increases, the VR-dPMSM periodically transitions between *1/3-PWM* and *3/3-PWM* modes, resulting in the so-called *2/3-PWM* operation mode, as shown in **Fig. 4(c)**. Eventually, at nominal speed, the system fully transitions into *3/3-PWM* mode, as depicted in **Fig. 4(d)**.

In the *3/3-PWM* mode, as expected, the quadrature current references no longer exhibit oscillations, since the DC link voltage u_{pn} is held constant and no power oscillation is required. Throughout all operating modes, the grid currents remain sinusoidal, confirming that PFC operation is consistently maintained.

It should be noted that across all PWM modes on the VR, the fundamental components of the dPMSM phase currents are electrically phase-shifted by $30°$, as shown in **Fig. 4(b.vii,c.vii,d.vii)**. This phase shift is an inherent characteristic of dual three-phase machines, resulting from the physical arrangement of the two winding sets [4].

The simulation results presented in **Fig. 4** clearly demonstrate that *1/3-PWM* operation on the VR can be successfully achieved with the support of the stacked inverters. This coordination, which we refer to as *synergetic control*, enables efficiency gains by reducing switching activity in the VR to one third of the grid period, resulting in up to 2/3 savings in VR switching losses.

The proposed control structure, shown in **Fig. 3**, ensures seamless operation and smooth transitions between all VR PWM modes (*1/3*, *2/3*, and *3/3*), which is verified with simulation results in **Fig. 4**. For completeness, it should also be noted that the inverse situation is theoretically possible, namely, achieving *1/3-PWM* operation on the stacked inverters at high speeds. In this case, the VR would regulate the DC link capacitor voltages to follow the line-to-line voltage envelope seen by the inverters. This scenario will be explored in detail in our future work.

V. Conclusion

This paper presented a novel Vienna rectifier-based dual three-phase PMSM (VR-dPMSM) drive system architecture, leveraging a Vienna rectifier (VR) to supply two stacked inverters for driving a dual three-phase machine. The proposed topology enables the exclusive use of $600\,\mathrm{V}$ semiconductor technology, allowing for efficient implementation with SiC or GaN devices. A synergetic control strategy was introduced that coordinates the VR and stacked inverters, enabling operation in a *1/3-PWM* mode in the VR that reduces VR's switching losses by up to two-thirds. The drive system also features dynamic DC link voltage adjustment by the VR, reduced DC link capacitance requirements that enable the use of film or ceramic capacitors, and power factor correction (PFC) operation. Time-domain simulations verified the effectiveness of the proposed concept across high and low operating speeds and demonstrated seamless transition between the PWM modes in the VR (1/3, 2/3, and 3/3).

Future work will focus on experimental validation of the VR-dPMSM drive system, the implementation of *1/3-PWM*

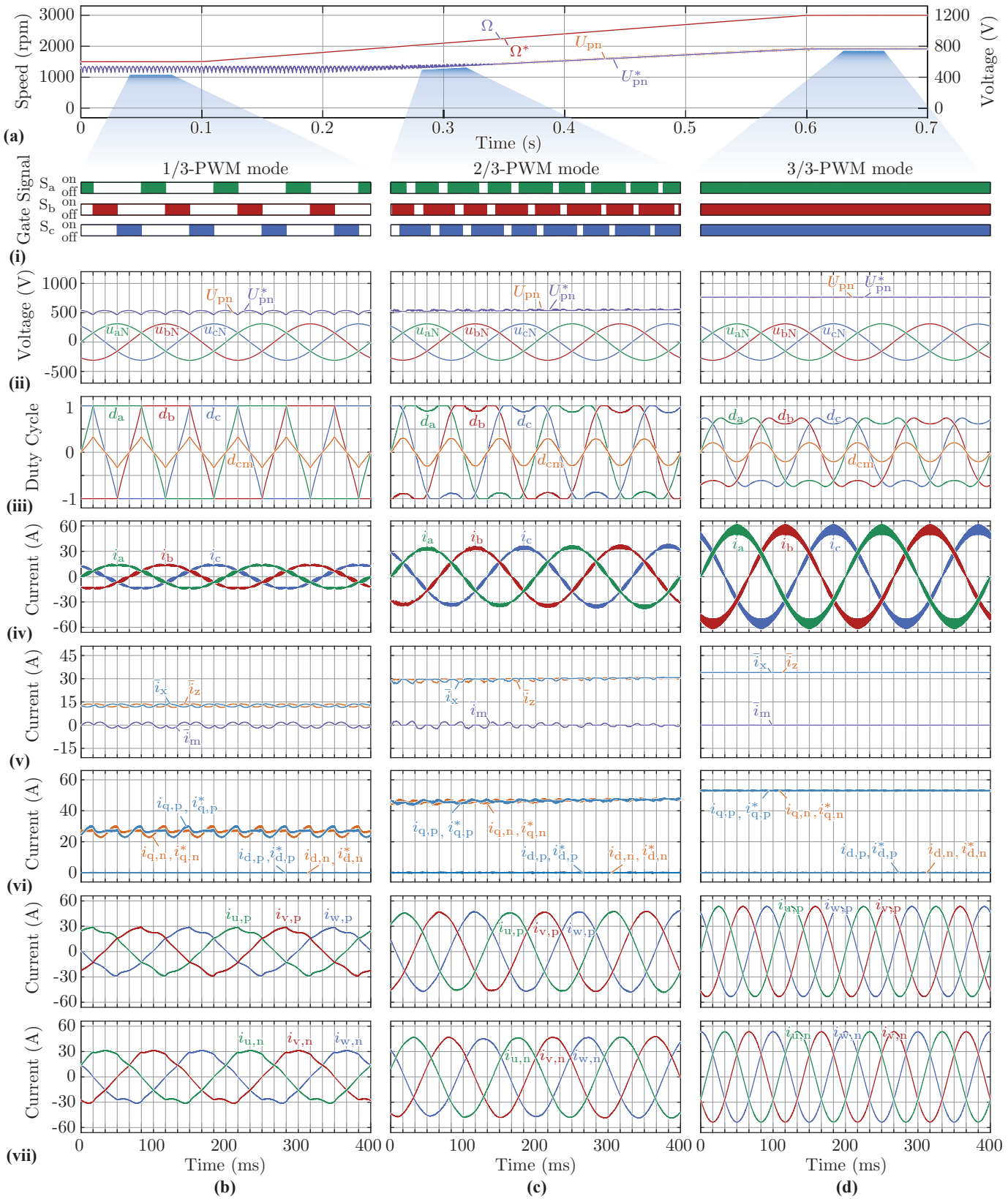

Fig. 4: Simulation waveforms of the VR-dPMSM drive system under V/f-based control. **(a)** Speed and DC-link voltage reference and response; **(b)** 1/3-PWM operation; **(c)** 2/3-PWM operation; and **(d)** 3/3-PWM operation. From top to bottom: **(i)** modulation method and VR gate signals, **(ii)** grid voltage, DC-link voltage, and its reference, **(iii)** VR duty cycles, **(iv)** grid currents, **(v)** local averages of the DC-link currents and midpoint current, **(vi)** references and responses of the d- and q-axis currents, and **(vii)** dPMSM phase currents.

operation in the stacked inverters at high speeds, and EMI analysis of the complete drive system.

APPENDIX

A. Expressions for u^*_{pn} Voltage Reference

The general expression that applies to any PWM operation mode (1/3, 2/3, or 3/3) is given as

$$u^*_{\mathrm{pn}} = \max\left(u^*_{\mathrm{pn},1/3},\, u^*_{\mathrm{pn},3/3},\, u^*_{\mathrm{pn},2/3,\mathrm{max}},\, u^*_{\mathrm{pn},2/3,\mathrm{min}}\right) \quad (5)$$

where

$$u^*_{\mathrm{pn},1/3} = u^*_{\mathrm{max}} - u^*_{\mathrm{min}} \quad (6)$$

and

$$u^*_{\mathrm{max}} = \max(u^*_{\bar{\mathrm{a}}}, u^*_{\bar{\mathrm{b}}}, u^*_{\bar{\mathrm{c}}}), \qquad u^*_{\mathrm{min}} = \min(u^*_{\bar{\mathrm{a}}}, u^*_{\bar{\mathrm{b}}}, u^*_{\bar{\mathrm{c}}}). \quad (7)$$

In *3/3-PWM* operation, the total DC link voltage reference u^*_{pn} is determined by the dPMSM speed and is given as

$$u^*_{\mathrm{pn},3/3} = 2\hat{U}_{\mathrm{nom}}\,\frac{\Omega^*}{\Omega_{\mathrm{nom}}}\cdot 2\cdot\gamma \quad (8)$$

where $\hat{U}_{\mathrm{nom}}$ is the peak of the nominal phase voltage of the dPMSM. Multiplying by 2 yields the required DC link voltage per inverter stage. This value is then scaled by the actual motor speed Ω^*, since $u^*_{\mathrm{pn},3/3}$ adapts with speed to maintain the DC link voltages as low as possible. It is further scaled by another factor of 2 to account for the total DC link voltage across both inverter stages, and by $\gamma = 1.2$ to provide a $20\,\%$ voltage margin ensuring proper current control across the motor inductances.

Further expressions for the *2/3-PWM* mode are given as

$$u^*_{\mathrm{pn},2/3,\mathrm{max}} = \frac{2}{1+\frac{3\hat{U}^2_{\mathrm{ac}}/2}{|u^*_{\mathrm{max}}||u^*_{\mathrm{pn},3/3}|}}\,u^*_{\mathrm{pn},1/3}, \quad (9)$$

$$u^*_{\mathrm{pn},2/3,\mathrm{min}} = \frac{2}{1+\frac{3\hat{U}^2_{\mathrm{ac}}/2}{|u^*_{\mathrm{min}}||u^*_{\mathrm{pn},3/3}|}}\,u^*_{\mathrm{pn},1/3}, \quad (10)$$

where $\hat{U}_{\mathrm{ac}}$ denotes the peak of the grid phase voltage [14].

B. Limits for u_{cm} Voltage

The common-mode voltage u_{cm} must be selected such that the total voltage applied to each phase remains within the DC link boundaries [12]:

$$-\frac{u_{\mathrm{pn}}}{2} \le \bar{u}_{\{\bar{a},\bar{b},\bar{c}\}} + u_{\mathrm{cm}} \le \frac{u_{\mathrm{pn}}}{2} \quad (11)$$

This condition ensures that the phase voltages, after adding the common-mode voltage, do not exceed the available DC link voltage.

The inequality in (11) can be rewritten using the expressions for u_{min} and u_{max} given in (7), yielding [14]:

$$-\frac{u_{\mathrm{pn}}}{2} - u_{\mathrm{min}} \le u_{\mathrm{cm}} \le \frac{u_{\mathrm{pn}}}{2} - u_{\mathrm{max}}. \quad (12)$$

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