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"Multi-Cell Current Source Inverter Topology for Modular Machine Drives"

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***Abstract*—This paper proposes a multi-cell current source inverter (mCSI) topology for modular machine drives. In contrast to the conventional series-stacked CSI approach, which requires $2n$ CSI cells for a machine with n segments, the proposed topology reduces the number of needed CSI cells to $n+1$, while retaining the key benefits of current-source operation. These include inherently smooth machine winding voltages and no per-phase current measurement. The derivation of the mCSI topology is explained and verified through time-domain simulations of a three-segment modular machine. The semiconductor stress distribution is analyzed, revealing that for a machine segment with peak phase voltage $\hat{U}$, the end-cell transistors of the mCSI experience maximum voltages of $\sqrt{3}\,\hat{U}$, while the mid-cell devices must withstand double of that $2\sqrt{3}\,\hat{U}$. Based on these findings, a comparative loss analysis between the mCSI and the conventional multi-cell voltage source inverter (mVSI) is performed. The results demonstrate that the mCSI achieves higher efficiencies and enables operation at higher switching frequencies compared to the mVSI. For instance, at 140 kHz, the mCSI reaches 99.76 % semiconductor efficiency, compared to 99.52 % of mVSI. These findings highlight the potential of the proposed mCSI topology as an attractive alternative for high-performance modular machine drives.**

***Index Terms*—Modular Multi-Segment Machines, Current Source Inverter (CSI), Multi-Cell Inverter, Monolithic Bidirectional Switch (MBDS)**

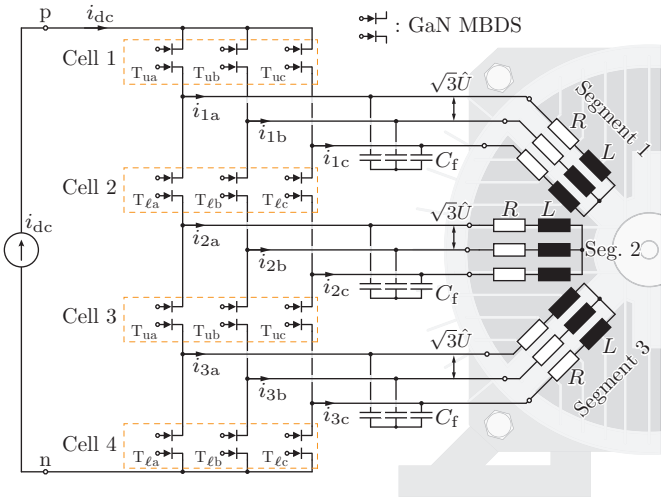

Fig. 1: Proposed multi-cell current source inverter (mCSI) topology for modular machine drives. The example corresponds to a three-segment machine ($n = 3$), requiring a total of $n_{\text{cell}} = n + 1 = 4$ CSI cells. The used semiconductors are GaN monolithic bidirectional switches (MBDSs) [7].

I. Introduction

Modular machine drives [1] are based on the principle that both the machine and the supplying converter (inverter) are modular. The machine is constructed with concentrated windings, allowing its stator and rotor to be divided into *segments* (often also named *sectors*) that can be assembled into a machine. Correspondingly, the supplying inverters are designed to interface with the appropriate machine segments. To the best of our knowledge, this drive concept has been known since the mid-1990s, originally motivated by the need to standardize motor parts for the growing power ratings of wind turbines. With identical stator and rotor segments, machines of different sizes could be realized, where each coil was equipped with its own dedicated converter [2], [3]. Around the same period, modular converter structures were also investigated for supplying traction induction machines with independent three-phase winding sets. In this case, the inverters were connected in series, enabling direct interfacing with the high-voltage single-phase grid without the need for an input transformer [4]–[6].

Converter segments in modular machine drives can be stacked in series such that the input converter handles the overall high power and high voltage, while each individual segment remains at a lower voltage level and processes only the power required for its respective machine sector [8]–[13]. This approach leverages the figure of merit of power semiconductors, since the converter segments can employ lower blocking-voltage devices compared to the input converter. Furthermore, such division of the machine converter into segments enables integration of this multi-segment converter[1] and the machine, as the converter can be physically distributed across the machine cross-section or around the machine [1], [9], [14]–[16]. In addition, modular drives offer improved reliability, since the failure of a single machine or converter segment

[1]In this paper, the term *multi-segment converter* is used. In the literature, such converters are also referred to as *multi-cell converter*. However, to avoid confusion, the term *cell* is reserved here exclusively for the CSI cell.

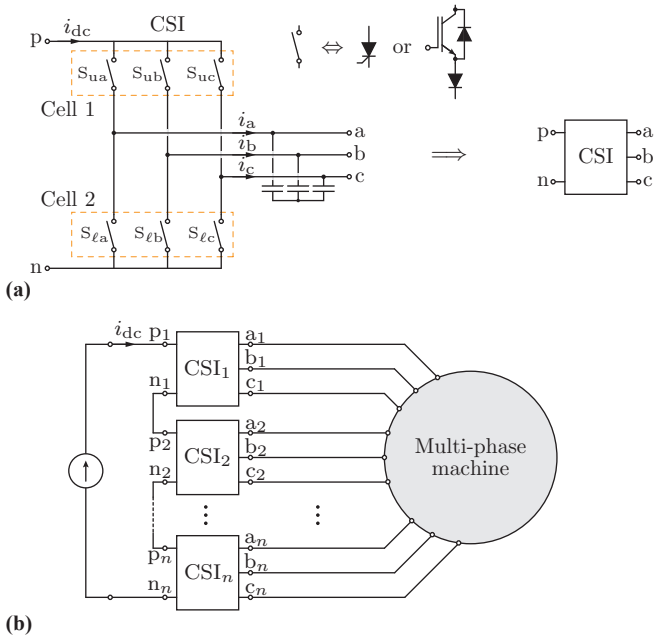

Fig. 2: Series stacking of CSIs as known in the literature [17]. **(a)** CSI topology with block notation, where the switch symbols indicate either thyristors or IGBTs connected in series with diodes. **(b)** General case of n series-stacked CSIs supplying multiple three-phase machine segments.

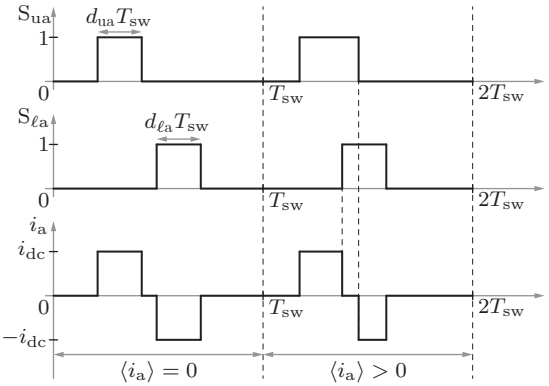

Fig. 3: Instantaneous gate signal and phase current waveforms illustrating how the average phase current is obtained according to (1). The pulse durations are determined by the duty cycles (d_{ua} and $d_{\ell a}$). Phase a is shown as an example, but the same principle applies to all other phases.

does not necessarily prevent the remaining segments from continuing operation [10], [12]. The main challenge associated with series stacking of voltage DC-link-based converters, however, lies in ensuring proper voltage balancing between the segments, which requires dedicated control strategies [11]. In addition, assuming the segments are voltage source inverters (VSIs), each VSI segment that supplies a dedicated machine sector requires current measurement to regulate the sector's phase currents. Consequently, each VSI segment also needs its own current controller and corresponding gate signals, which significantly increases the overall component count and system complexity.

On the other hand, a current source inverter (CSI) can be stacked in series and used to supply machine segments, a common approach particularly in high-power drive systems such as those employed in wind turbines [17]–[20], as illustrated in **Fig. 2**. Historically, series stacking of CSIs was already applied in thyristor-based converters with six-step commutation, where the resulting low-frequency torque ripple of the machine was problematic. By supplying two sets of three-phase windings with two series-stacked thyristor converters, the number of steps was effectively doubled, thereby shifting the torque oscillation frequency to a higher range and avoiding issues such as mechanical resonances [21]. Later, even PWM-operated series-stacked thyristor CSIs were proposed for supplying individual machine phases [22]. Remarkably, such thyristor-based CSI drives are still in use today in megawatt-scale applications [23].

Advantageously, series stacking of CSIs, as conceptually illustrated in **Fig. 2(b)**, addresses issues typical for VSI-based stacked segments, such as voltage stability and balancing between segments. In addition, CSI segments provide a smooth voltage across the motor windings compared to the pulsed voltages inherent to VSIs. Another advantage is that CSI segments do not require dedicated current measurement for each machine segment, since the current is directly modulated and the desired phase currents for the machine segments are obtained by setting the appropriate duty cycles. Assuming symmetric machine segments, the same gate signals can be applied across all segments. For example, if six gate signals are required for a three-phase CSI segment, the same six signals can be used for each segment of a modular machine. A slight drawback of the CSI approach is that each segment requires either a MOSFET in series with a diode or a bidirectional switch (BDS), in contrast to the single MOSFET typically sufficient for a VSI segment.

Each CSI consists of two CSI cells, for example: Cell 1, containing S_{ua}, S_{ub}, and S_{uc}, and Cell 2, containing $S_{\ell a}$, $S_{\ell b}$, and $S_{\ell c}$, see **Fig. 2(a)**. Consequently, to realize a modular machine with n segments by stacking CSIs (see **Fig. 2(b)**), the total number of CSI cells required is $n_{cell} = 2\,n$. This paper proposes a multi-cell current source inverter (mCSI) topology for modular machine drives that employs series stacking of CSI cells, but reduces the requirement of total number of CSI cells to $n_{cell} = n + 1$, while retaining all advantages of conventional series-stacked CSIs: no stability or voltage-balancing issues, smooth voltage across the machine segment windings, no need for phase current measurements, and gate signals that only need to be generated for two CSI cells and can be reused for the others. The proposed mCSI topology is illustrated in **Fig. 1**, and its derivation and operation are explained in detail in the following sections.

II. mCSI Topology Derivation

For the derivation of the mCSI topology, it is important to review the modulation principle of CSIs [24]. Unlike VSIs,

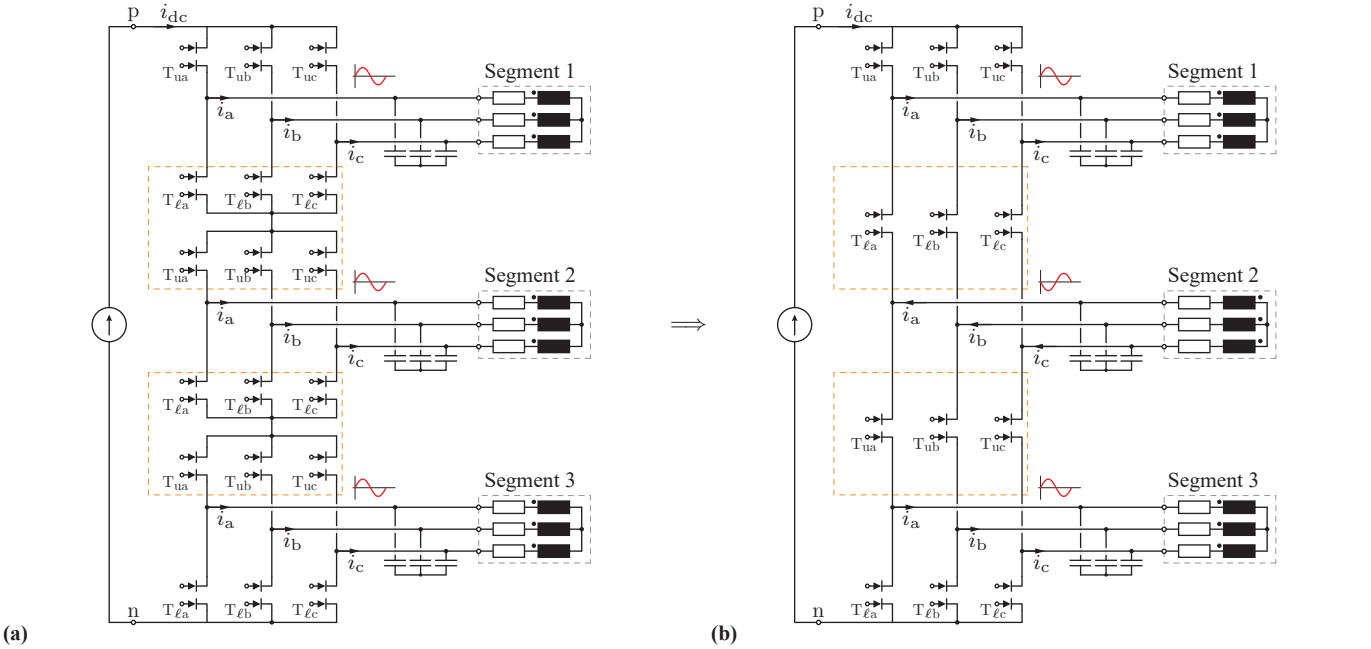

Fig. 4: Derivation of the mCSI topology using a three-segment machine example ($n = 3$). **(a)** Conventional series stacking of CSIs, requiring three CSIs or a total of $n_{\text{cell}} = 2n = 6$ three-phase CSI cells. **(b)** Proposed mCSI, where each pair of upper and lower CSI cells is replaced by a single CSI cell, reducing the total requirement to $n_{\text{cell}} = n + 1 = 4$.

which are modulated per half-bridge, CSIs are modulated per cell. Therefore, for example, in **Fig. 2(a)**, a separate modulator is required for each cell [24], handling the upper duty cycles d_{ua}, d_{ub}, d_{uc}, and handling lower duty cycles $d_{\ell\text{a}}$, $d_{\ell\text{b}}$, $d_{\ell\text{c}}$. To ensure continuity of i_{dc}, the duty cycles must sum to unity, i.e., $d_{\text{ua}} + d_{\text{ub}} + d_{\text{uc}} = 1$ and $d_{\ell\text{a}} + d_{\ell\text{b}} + d_{\ell\text{c}} = 1$, and at any instant only one switch within a cell may be on. The number of duty cycles per CSI cell equals the number of CSI phases. Although the CSI modulator is used per CSI cell, the average phase current $\langle i_{\text{a}} \rangle$ depends on the duty cycles of both the upper and lower cells, and is determined by the difference between their respective duty cycles:

$$\langle i_{\text{a}} \rangle = i_{\text{dc}} \left(d_{\text{ua}} - d_{\ell\text{a}} \right), \tag{1}$$

where $\langle \cdot \rangle$ denotes averaging over the switching period T_{sw}. Equation (1) holds under the assumption that i_{dc} remains constant during T_{sw}. A similar relation applies to phases b and c, $\langle i_{\text{b}} \rangle = i_{\text{dc}} \left(d_{\text{ub}} - d_{\ell\text{b}} \right)$ and $\langle i_{\text{c}} \rangle = i_{\text{dc}} \left(d_{\text{uc}} - d_{\ell\text{c}} \right)$, as well as to any additional phases in the case of CSIs with more than three phases. If we observe the instantaneous values, the currents produced by CSI switching are pulses with i_{dc} peak and duration determined by the duty cycles, see **Fig. 3**. These pulses contribute to the averaged value of the phase currents. For example, when only the upper switch is on, the respective phase current is positive and equal to i_{dc}; when only the lower switch is on, the current is negative and equal to $-i_{\text{dc}}$; and when both are on, the current is zero. This behavior is illustrated in **Fig. 3**, showing how the average current follows directly from (1) by taking the average value of those pulses within the switching period T_{sw}.

Control of the series-stacked CSIs in **Fig. 4(a)** is performed per CSI. Since the machine segments are assumed to require identical three-phase current systems, the gate signals for the upper and lower cells can be shared among the CSIs, provided that no decoupled switching is required (e.g., for common-mode noise compensation by carrier phase shifting). It should be emphasized again that the average phase current depends solely on the difference between the duty cycles of the upper and lower cells associated with the considered machine segment. If we now replace the selected upper and lower cells (encircled in **Fig. 4(a)**) with a single CSI cell, the resulting topology is shown in **Fig. 4(b)**. The key question then becomes how to control this new topology.

To illustrate the principle, we proceed segment by segment. For segment 1 of the proposed topology in **Fig. 4(b)**, the same duty cycles can be used for the upper cell switches T_{ua}, T_{ub}, T_{uc} and the lower switches $\text{T}_{\ell\text{a}}$, $\text{T}_{\ell\text{b}}$, $\text{T}_{\ell\text{c}}$ as in the conventional series-stacked CSI of **Fig. 4(a)**.

For segment 2, the duty cycles of the upper CSI cell relative to this segment are already defined, as they correspond to the lower-cell duty cycles of segment 1. Therefore, for the lower cell of segment 2, it is logical to apply the duty cycles corresponding to the upper duty cycles of segment 1. This results in the same magnitude of the phase currents but with opposite sign, since flipping the upper and lower duty cycles inverts the averaged current:

$$i_{\text{dc}} \left(d_{\ell\text{a}} - d_{\text{ua}} \right) = -\langle i_{\text{a}} \rangle, \tag{2}$$

for segment 2 of the proposed topology in **Fig. 4(b)**. The inverted current direction does not pose an issue for the machine,

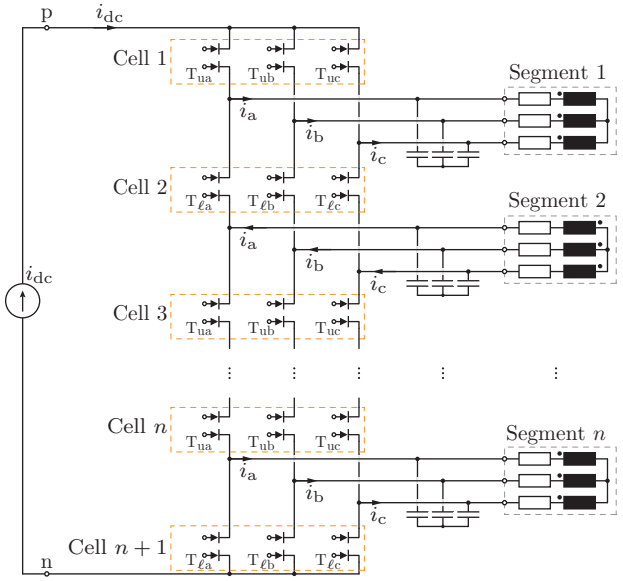

Fig. 5: Schematic of the proposed mCSI for general case supplying n machine segments, requiring a total of $n_{\text{cell}} = n + 1$ CSI cells.

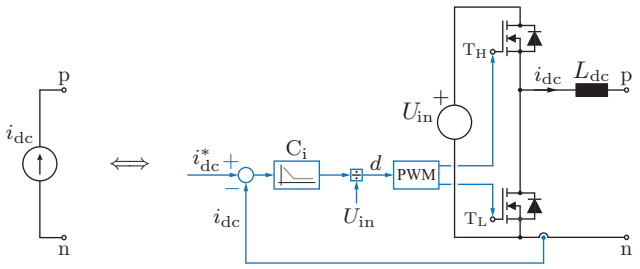

Fig. 6: Realization of the current source in the time-domain simulation used to supply the mCSI driving the three-segment machine from **Fig. 1**. The input voltage is $U_{\text{in}} = 800\,\text{V}$, the switching frequency is $48\,\text{kHz}$, and the DC-link inductor is $L_{\text{dc}} = 1.5\,\text{mH}$.

Parameter	Symbol	Value
mCSI		
Output capacitance	C_{f}	$0.1\,\mu\text{F}$
Switching frequency	f_{sw}	$140\,\text{kHz}$
Modulation index	m	1
Modular PMSM		
Number of segments	n	3
Phase resistance	R	$0.1\,\Omega$
Phase inductance	L	$1\,\text{mH}$
Flux linkage	$\hat{\Psi}$	$80\,\text{mWb}$
Number of pole pairs	p	3
Moment of inertia	J	$0.001\,\text{kgm}^2$
Nominal mech. power	P_{mech}	$9.9\,\text{kW}$
Nominal mech. speed	n_{mech}	$3000\,\text{rpm}$

TABLE I: Simulation Parameters.

as it can be compensated simply by reversing the winding connection, as indicated by the polarity dots in **Fig. 4(b)**.

For segment 3, the duty cycles of the upper CSI cell are again predefined. The lower cell of segment 3 can therefore reuse the same duty cycles as the lower cell of segment 1. In this case, the current direction remains unchanged.

The proposed topology shown in **Fig. 4(b)** is referred to as the *multi-cell current source inverter* (mCSI) topology for modular machine drives.

A similar situation, where the duty cycles of a single cell influence two AC loads, can be found in the so-called nine-switch CSI topology discussed in [25], [26].

For a general number of segments n, the proposed mCSI is realized with $n_{\text{cell}} = n + 1$ CSI cells, as illustrated in **Fig. 5**. Regardless of the number of segments n, the mCSI requires only six duty cycles and, consequently, six gate signals (assuming a single gate signal per MBDS, which can be achieved using self-switching gate drivers [27] or by employing a cascode configuration of an MBDS with a low-voltage Schottky diode [28]) to be controlled. This reduction is possible because identical currents are assumed for all machine segments. The following section clarifies the modulation of the mCSI by analyzing the duty cycle and current waveforms.

III. mCSI Operation Example

The operating principles of the mCSI discussed in **Sec. II** are exemplified here through waveforms obtained from time-domain circuit simulations. The simulation schematic is shown in **Fig. 1**, where, instead of using an ideal current source, a more realistic implementation is adopted by employing a current-controlled buck converter, as depicted in **Fig. 6**. The parameter values used in the simulation for the mCSI and the modular PMSM from **Fig. 1** are listed in **Tab. I**.

The steady-state waveforms from the time-domain transient simulation for one fundamental period are shown in **Fig. 7**. The duty cycles of the *upper* CSI cell, d_{ua}, d_{ub}, d_{uc}, and the *lower* CSI cell, $d_{\ell\text{a}}$, $d_{\ell\text{b}}$, $d_{\ell\text{c}}$, are depicted in **Fig. 7(a,b)**. The modulation index, defined as $m = \hat{I}/i_{\text{dc}}$, i.e., the ratio of the AC current peak $\hat{I}$ to the DC-link current i_{dc}, is set to a constant value of $m = 1$, corresponding to the so-called equivalent DC machine operation (E-DCM) [29]. The duty cycles d_{ua}, d_{ub}, d_{uc} and $d_{\ell\text{a}}$, $d_{\ell\text{b}}$, $d_{\ell\text{c}}$ are obtained using the CSI modulation method from [24], under the assumption of equal distribution of the *excess duty* cycle among the phases.

According to (1), the difference between the upper and lower duty cycles defines the output phase currents. This difference is shown in **Fig. 7(c)**, which, for $m = 1$, alternates between -1 and 1. It can be observed that this duty cycle difference directly determines the phase currents, as the phase currents of segment 1 follow the sinusoidal shape of the duty cycle difference. As emphasized in **Fig. 1**, for segment 1 the upper duty cycles are d_{ua}, d_{ub}, and d_{uc}, while the lower duty cycles are $d_{\ell\text{a}}$, $d_{\ell\text{b}}$, and $d_{\ell\text{c}}$. Therefore, in accordance with (1), exactly the duty cycle difference shown in **Fig. 7(c)** defines the phase currents of segment 1, depicted in **Fig. 7(d)**. The DC-link current is $i_{\text{dc}} = 23\,\text{A}$ with a peak-to-peak high-frequency ripple of $2.8\,\text{A}$.

As shown in **Fig. 1**, for segment 2 the upper duty cycles are $d_{\ell\text{a}}$, $d_{\ell\text{b}}$, and $d_{\ell\text{c}}$, while the lower duty cycles are d_{ua}, d_{ub}, and d_{uc}. Consequently, the phase currents generated by the mCSI for segment 2 have the same magnitude as those

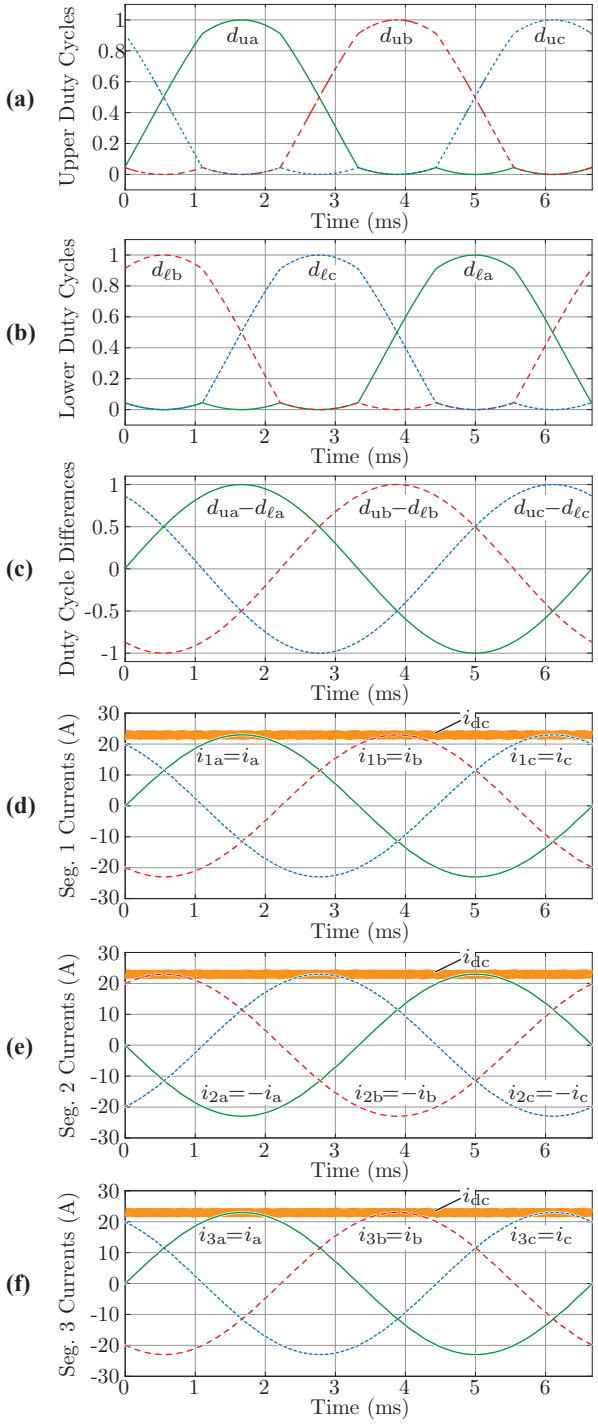

Fig. 7: Transient time-domain simulation showing the results reached in steady state for the three-segment mCSI-supplied machine from **Fig. 1** at nominal power 7.5 kW and speed 3000 rpm. The shown waveforms correspond to the nominal power and speed operating point. Simulation parameters are listed in **Tab. I**. The plots show: **(a)** duty cycles of the *upper* CSI cell, **(b)** duty cycles of the *lower* CSI cell, **(c)** difference between the upper and lower CSI cell duty cycles, **(d)** phase currents of segment 1, **(e)** phase currents of segment 2 (opposite in direction to those of segment 1), **(f)** phase currents of segment 3 (same direction as segment 1, opposite to segment 2), and the DC link current.

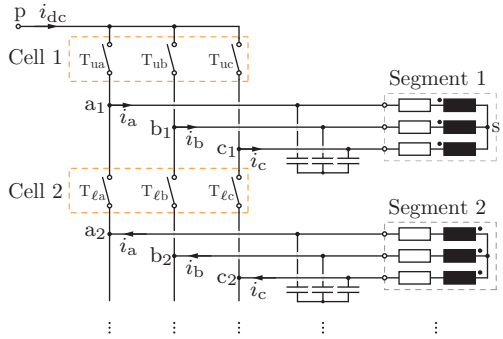

Fig. 8: Node notation used for explaining the waveforms for phase voltages, line-to-line voltages, and voltages over the switches in **Fig. 9**.

of segment 1, but flow in the opposite direction, see (2) and **Fig. 7(e)**. To account for this, the windings of segment 2 must be connected with opposite polarity compared to those of segment 1, as indicated in **Fig. 4(b)** with dots on the inductance. For segment 3, the situation again matches that of segment 1, resulting in phase currents with the same direction, as confirmed by the waveforms in **Fig. 7(f)**. For more than three segments, this alternating current direction would have repeated systematically for all subsequent segments.

Finally, with six duty cycles, the mCSI defines the three-phase currents i_a, i_b, and i_c, which are supplied to the modular machine segments. The only requirement is to account for the current direction, which depends on whether the upper or lower duty cycles are applied to a given CSI cell. These assignments must alternate from cell to cell. With this principle, the same six duty cycles can be used to control the mCSI for any number of (three-phase) machine segments.

For the nominal operating point, corresponding to a mechanical power of 7.5 kW and a nominal speed of 3000 rpm, and with the phase current waveforms shown in **Fig. 7**, the resulting phase voltages across the machine and the switches of the mCSI are presented in **Fig. 9**. Voltages are denoted according to the node notation introduced in **Fig. 8**. For example, the voltage between nodes a_1 and s is expressed as $u_{a1,s} = v_{a1} - v_s$, representing the potential difference between these two nodes.

The goal of this analysis is to determine the required blocking voltage of the semiconductors in the mCSI, so that we can derive an analytical relation between the blocking voltage and the peak phase voltages of the machine segments. We begin by examining the segment phase voltages, as shown for segment 1 in **Fig. 9(a)**. Since blocking voltages in the mCSI are primarily governed by line-to-line voltages, the waveforms for segments 1 and 2 are depicted in **Fig. 9(b,c)**.

First, consider CSI cell 1, which is connected to the positive rail. From Kirchhoff's voltage law, it follows that the switches in this cell experience a maximum blocking voltage equal to the peak line-to-line voltage. For a cell located between other cells, such as cell 2 (see **Fig. 8**), Kirchhoff's voltage law shows that the maximum blocking voltage across its switches is twice the peak line-to-line voltage, i.e., twice the stress experienced

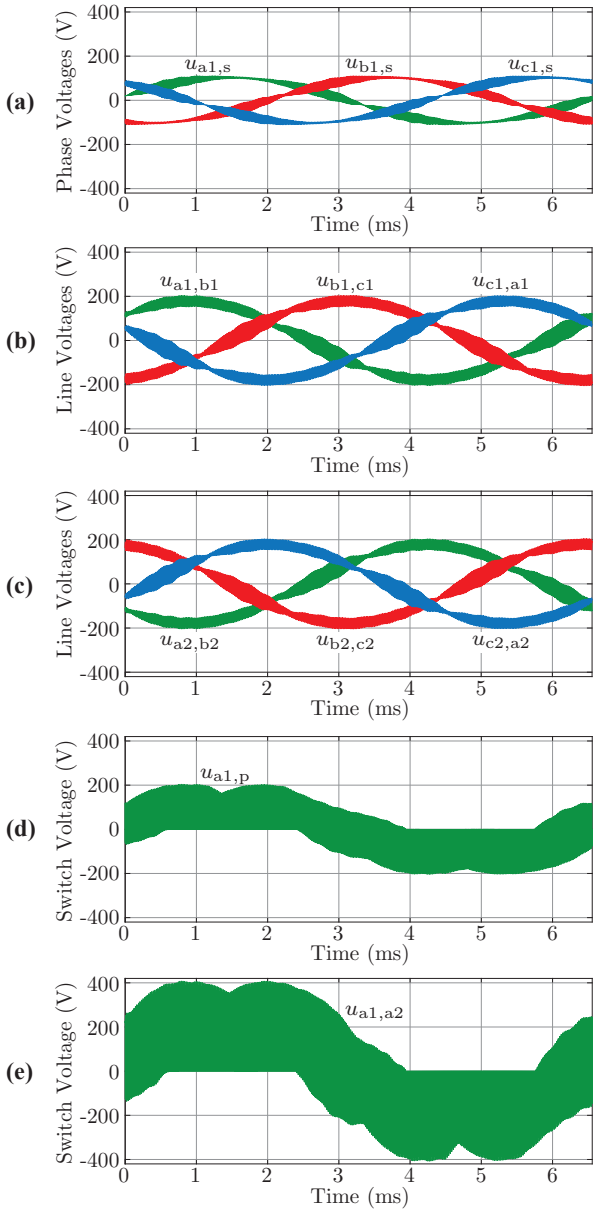

Fig. 9: Instantaneous voltages across capacitors and switches: **(a)** machine phase voltage, e.g., $u_{\mathrm{a1,s}} = v_{\mathrm{a1}} - v_{\mathrm{s}}$ (see **Fig. 8** for node notation); **(b)** line-to-line voltages of segment 1; **(c)** line-to-line voltages of segment 2; **(d)** voltage across the switch of the first phase in cell 1 connected to the positive rail; **(e)** voltage across the switch of the first phase in the mid cell 2.

by the switches of cell 1 connected to the positive rail. This is confirmed by the waveform of the instantaneous voltage $u_{\mathrm{a1,a2}}$ in **Fig. 9(a)**.

Therefore, the first and last cells of the mCSI, i.e., those connected to the positive and negative rails, experience a switch blocking voltage equal to the maximum line-to-line voltage, while all intermediate cells are subjected to twice this value. Assuming the phase voltage peak is $\hat{U}$ and neglecting the high-frequency voltage ripple, the devices in the first and last (end) cells must withstand blocking voltages greater

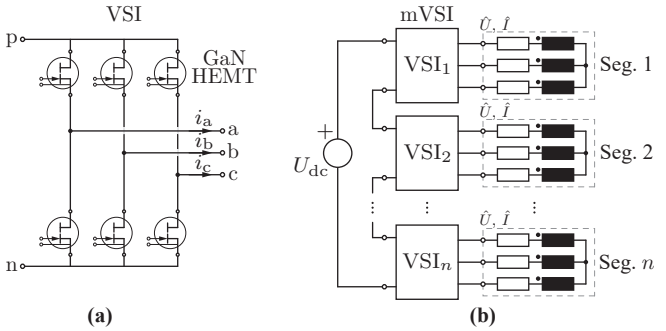

Fig. 10: (a) Two-level voltage source inverter (VSI) with GaN HEMT transistors. **(b)** Series-stacked VSIs, i.e., the multi-cell voltage source inverter (mVSI) topology [12] for modular machine drives.

Key Quantities	**mVSI**	**mCSI**	
		end	mid
Device type	GaN HEMT	GaN MBDS	
Num. of segments (n)	3	3	
Num. of phases per seg.	3	3	
Num. of devices	$6n$	6	$3(n-1)$
Rated voltage (U_{rated})	$2\hat{U}$	$\sqrt{3}\hat{U}$	$2\sqrt{3}\hat{U}$
Dev. ON-state res. ($R_{\mathrm{ds,on}}$)	R_{on}	R_{end}	R_{mid}

TABLE II: mVSI and mCSI Key Quantities.

than $\sqrt{3}\,\hat{U}$. The devices in the intermediate (mid) cells must withstand blocking voltages greater than $2\sqrt{3}\,\hat{U}$. This result will be used in the next section to compare the figure of merit of the proposed mCSI topology with that of the conventional multi-cell VSI (mVSI) topology for modular machine drives.

IV. mCSI and mVSI Comparison

In this section, the proposed mCSI topology (see **Fig. 5**) is compared with the well-known multi-cell voltage source inverter (mVSI) topology (see **Fig. 10**). The corresponding key quantities for both topologies are summarized in **Tab. II**. Each inverter (mVSI and mCSI) is assumed to supply a total power of

$$P_{\mathrm{el}} = n\,\frac{3}{2}\hat{U}\hat{I}, \tag{3}$$

to the machine, where $\hat{U}$ and $\hat{I}$ denote the peak phase voltage and current per segment, respectively, and n is the number of machine segments. The expressions are kept general in terms of n, while the final numerical results are evaluated for $n = 3$. The peak phase voltage is set to $\hat{U} = 100\,\mathrm{V}$, which corresponds to a peak phase current of $\hat{I} = 23\,\mathrm{A}$ and results in a total electrical output power of $P_{\mathrm{el}} = 10.35\,\mathrm{kW}$ delivered to the machine.

We compare the achievable efficiencies of the mVSI and mCSI when delivering P_{el}, calculated as

$$\eta_{\{\mathrm{mVSI,mCSI}\}} = \frac{P_{\mathrm{el}} - P_{\mathrm{semi},\{\mathrm{mVSI,mCSI}\}}}{P_{\mathrm{el}}}, \tag{4}$$

where $P_{\mathrm{semi,mVSI}}$ and $P_{\mathrm{semi,mCSI}}$ denote the total semiconductor losses of the mVSI and mCSI, respectively. These losses are composed of conduction and switching losses:

$$\begin{aligned} P_{\mathrm{semi,mVSI}} &= P_{\mathrm{cond,mVSI}} + P_{\mathrm{sw,mVSI}}, \\ P_{\mathrm{semi,mCSI}} &= P_{\mathrm{cond,mCSI}} + P_{\mathrm{sw,mCSI}}, \end{aligned} \tag{5}$$

with the detailed calculation explained in the following.

A. Conduction Losses

The conduction losses of the mVSI are given by

$$P_{\mathrm{cond,mVSI}} = 6n\, R_{\mathrm{on}} \left(\tfrac{\hat{I}}{2}\right)^2, \tag{6}$$

where $6n$ is the total number of GaN HEMT transistors in the mVSI, R_{on} is their ON-state drain-source resistance, and $\hat{I}/2$ is the RMS current through each transistor.

The conduction losses of the mCSI are given by

$$P_{\mathrm{cond,mCSI}} = \left(6\, R_{\mathrm{end}} + 3(n-1)\, R_{\mathrm{mid}}\right) \left(\tfrac{\hat{I}}{\sqrt{3}}\right)^2, \tag{7}$$

where 6 corresponds to the number of GaN MBDS end transistors in the mCSI, i.e., those in the CSI cells connected to the positive and negative DC-link rails, $3(n-1)$ is the number of mid transistors, R_{end} and R_{mid} are their respective ON-state drain-source resistances, and $\hat{I}/\sqrt{3}$ is the RMS current through each transistor.

Next, the ON-state drain-source resistance is related to the device chip area using the area-normalized ON-resistance as

$$r(U_{\mathrm{rated}}) = R_{\mathrm{ds,on}}\, a_{\mathrm{chip}} = \rho U_{\mathrm{rated}}^{\gamma}, \tag{8}$$

where a_{chip} is the chip area per device, and $\rho = 0.26$ and $\gamma = 1.1$ [30] are fitting parameters of the device technology. For this comparison, the device rated voltage is assumed to be equal to the maximum voltage stress across the device. Consequently, the rated voltages U_{rated} differ between the mVSI and mCSI, resulting in different ON-state resistances.

For the mVSI, the rated voltage is $U_{\mathrm{rated}} = 2\hat{U}$, which yields

$$R_{\mathrm{on}} = \frac{\rho(2\hat{U})^{\gamma}}{a_{\mathrm{mVSI}}}, \tag{9}$$

where the total chip area for the mVSI is

$$A_{\mathrm{tot,mVSI}} = 6n\, a_{\mathrm{mVSI}}. \tag{10}$$

For the mCSI, the rated voltages of the end and mid devices are $\sqrt{3}\,\hat{U}$ and $2\sqrt{3}\,\hat{U}$, respectively, resulting in the ON-state resistances

$$R_{\mathrm{end}} = \frac{\rho(\sqrt{3}\,\hat{U})^{\gamma}}{a_{\mathrm{end}}}, \quad R_{\mathrm{mid}} = \frac{\rho(2\sqrt{3}\,\hat{U})^{\gamma}}{a_{\mathrm{mid}}}, \tag{11}$$

where the total chip area of the end transistors is $A_{\mathrm{end}} = 6a_{\mathrm{end}}$ and that of the mid transistors is $A_{\mathrm{mid}} = 3(n-1)a_{\mathrm{mid}}$. The total chip area for the mCSI is therefore

$$A_{\mathrm{tot,mCSI}} = A_{\mathrm{end}} + A_{\mathrm{mid}}. \tag{12}$$

B. Switching Losses

The switching losses of the mVSI can be estimated using a single value of the output charge $Q_{\mathrm{oss}}(U_{\mathrm{dc}})$ corresponding to the DC-link voltage level, yielding $f_{\mathrm{sw}} Q_{\mathrm{oss}}(U_{\mathrm{dc}}) U_{\mathrm{dc}}$. Assuming $U_{\mathrm{dc}} = U_{\mathrm{rated}} = 2\hat{U}$, the switching losses (considering only capacitive losses, i.e., $\mathrm{d}v/\mathrm{d}t$-independent losses) are

$$P_{\mathrm{sw,mVSI}} = 3n\, f_{\mathrm{sw}} Q_{\mathrm{oss}}(2\hat{U})\, 2\hat{U}, \tag{13}$$

where $3n$ is the total number of half-bridges in the mVSI, since hard-switching losses occur in either the high-side or the low-side switch of each half-bridge, and f_{sw} is the switching frequency.

The output charge at the rated voltage can be obtained from the figure of merit [12], defined as

$$\mathrm{FoM}(U_{\mathrm{rated}}) = \frac{1}{R_{\mathrm{ds,on}}(U_{\mathrm{rated}})\, Q_{\mathrm{oss}}(U_{\mathrm{rated}})} = \alpha\, U_{\mathrm{rated}}^{\kappa}, \tag{14}$$

where $\alpha = 1.63 \times 10^{12}$ and $\kappa = -1.4$, which yields the output charge at the rated voltage as

$$Q_{\mathrm{oss}}(U_{\mathrm{rated}}) = \frac{U_{\mathrm{rated}}^{-\kappa}}{\alpha\, R_{\mathrm{ds,on}}(U_{\mathrm{rated}})}. \tag{15}$$

Accordingly, for the mVSI, the output charge is

$$Q_{\mathrm{oss}}(2\hat{U}) = \frac{(2\hat{U})^{-\kappa}}{\alpha\, R_{\mathrm{on}}},$$

where the ON-state resistance R_{on} of the mVSI is given in (9).

The calculation of switching losses for the mCSI is more involved, since the voltage across the transistors varies over time. Assuming the switching frequency is much higher than the fundamental frequency, the voltage across the devices can be considered constant within each switching period. To obtain the total switching losses over one fundamental period, the losses must be integrated over the instantaneous output voltages, yielding

$$\begin{aligned} P_{\mathrm{sw,mCSI}} = 6\, \frac{1}{2\pi} \int_0^{2\pi} & f_{\mathrm{sw}}\, q_{\mathrm{oss}}(u_{\mathrm{end}}(\theta))\, u_{\mathrm{end}}(\theta)\, \mathrm{d}\theta \\ & + 3(n-1)\, \frac{1}{2\pi} \int_0^{2\pi} f_{\mathrm{sw}}\, q_{\mathrm{oss}}(u_{\mathrm{mid}}(\theta))\, u_{\mathrm{mid}}(\theta)\, \mathrm{d}\theta, \end{aligned} \tag{16}$$

where the output charge as a function of voltage is expressed as

$$q_{\mathrm{oss}}(u) = \frac{Q_{\mathrm{oss}}(U_{\mathrm{rated}})}{U_{\mathrm{rated}}^{1-\mu}}\, u^{1-\mu}. \tag{17}$$

The dependence $u^{1-\mu}$ is based on the generalized junction-capacitance model [31], with $\mu = 0.5$. For comparison, $\mu = 0.48$ was experimentally verified in [32] for SiC technology.

The u_{end} and u_{mid} voltage waveforms used in (16) are shown in **Fig. 11** and represent the voltages that determine q_{oss} for the transistors contributing to hard-switching losses and depend on the switching sequences ① and ② that are denoted in **Fig. 11**.

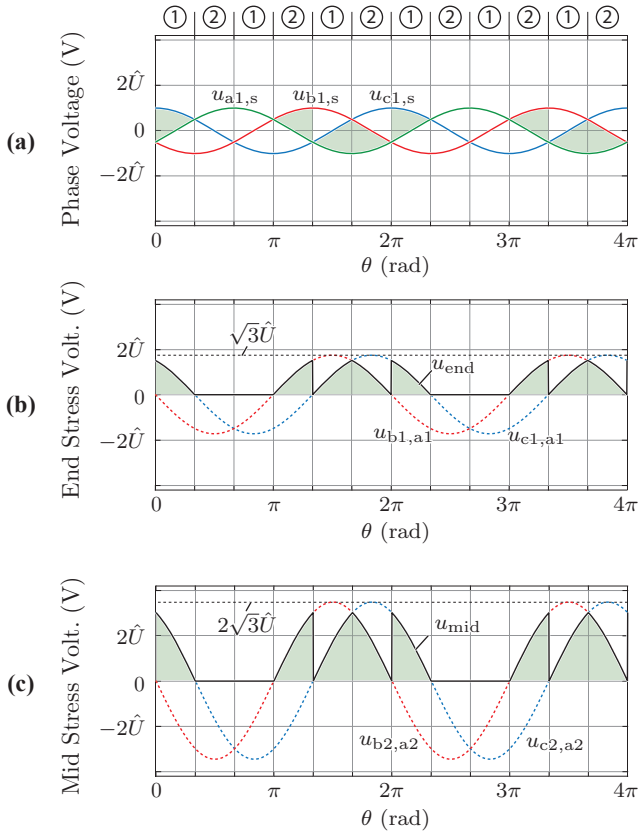

Fig. 11: Voltage waveforms used for the switching-loss calculation of the mCSI: **(a)** phase voltages of segment 1, **(b)** end-device voltage u_{end}, and **(c)** mid-device voltage u_{mid}, as used in (16). The circled numbers indicate the commutation sequence within the cells, where ① corresponds to the a→b→c→a sequence, and ② corresponds to the c→b→a→c sequence.

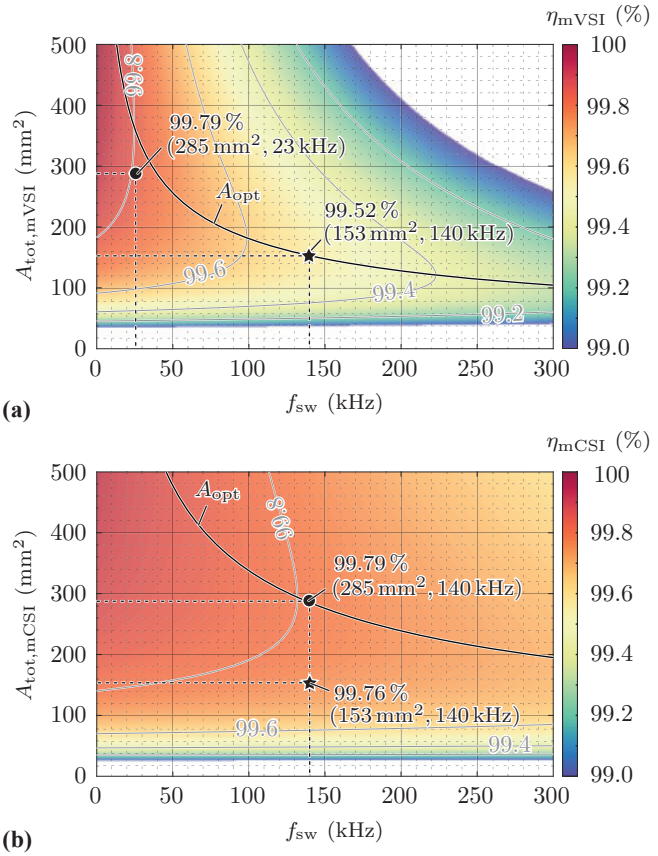

Fig. 12: Efficiency of **(a)** the mVSI topology and **(b)** the mCSI topology, calculated using (4).

C. Comparison

To compare the mVSI and mCSI, we evaluate the efficiencies η_{mVSI} and η_{mCSI} as defined in (4). In addition to the specification parameters introduced earlier (see the first paragraph of this section), we perform a numerical sweep of the switching frequency f_{sw} in 1 kHz steps and of the total chip areas $A_{\mathrm{tot,mVSI}}$ and $A_{\mathrm{tot,mCSI}}$ in 1 mm^2 steps.

For the mCSI, at each sweep point of $A_{\mathrm{tot,mCSI}}$, the factor x numerically solved to determine the distribution of chip area between the end and mid devices, such that $A_{\mathrm{end}} = xA_{\mathrm{tot,mCSI}}$ and $A_{\mathrm{mid}} = (1-x)A_{\mathrm{tot,mCSI}}$. The value of x that minimizes the total semiconductor losses $P_{\mathrm{semi,mCSI}}$ is then selected, and only this optimal case is considered.

The comparison results are presented in **Fig. 12**, showing that the mCSI achieves higher efficiencies at higher switching frequencies compared to the mVSI. For example, at $f_{\mathrm{sw}} = 140\,\mathrm{kHz}$ and assuming the same total chip area, the mCSI reaches an efficiency of $\eta_{\mathrm{mCSI}} = 99.76\,\%$, compared to $\eta_{\mathrm{mVSI}} = 99.52\,\%$ for the mVSI. It should be noted that the chip areas of the mVSI and mCSI correspond to different voltage levels, as discussed in this section.

V. Conclusions

This paper introduced a novel multi-cell current source inverter (mCSI) topology for modular machine drives. The derivation of the topology showed that only $n+1$ CSI cells are required for a machine with n segments, which is almost half the number of cells ($2n$) compared to the conventional series-stacked CSI approach. The modulation scheme was discussed, demonstrating how six duty cycles are sufficient to supply any number of three-phase machine segments, with alternating current directions handled by proper winding connections.

A detailed analysis of device blocking voltages revealed that end-cell devices must withstand at least $\sqrt{3}\,\hat{U}$, while mid-cell devices must withstand $2\sqrt{3}\,\hat{U}$. This information was used to establish a fair figure-of-merit based loss comparison with the conventional multi-cell VSI (mVSI). The comparison shows that the mCSI consistently outperforms the mVSI in terms of efficiency, particularly at higher switching frequencies, while also eliminating the need for per-phase current measurement and enabling simpler gate signal reuse across machine segments.

Future work will include experimental validation of the mCSI topology on a hardware demonstrator.

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