A Switch-per-Phase PWM Current Source Converter Topology for Variable Reluctance Motor Drives

Takanobu Ohno[1], Michael Haider, Keitaro Kawarazaki[2], Nobukazu Hoshi[2] and, Spasoje Mirić[1]
[1] Drives and Energy Systems Laboratory, University of Innsbruck, 6020 Innsbruck, Austria
[2] Dept. of Electrical Engineering, Tokyo University of Science, Chiba, Japan
Email: spasoje.miric@uibk.ac.at

***Abstract*—Variable reluctance motors (VRMs) are an attractive solution for drive systems due to their simple construction and the absence of permanent magnets. Their torque is generated by an attractive force between stator and rotor teeth, resulting in inherently unipolar phase currents. This property allows for simplified converter topologies compared to machines requiring bipolar current waveforms. While numerous VRM converter topologies have been proposed, they are predominantly based on voltage-source DC links, which impose high-frequency pulsed voltages across the motor windings. In this paper, we propose a current-source converter (CSC) topology tailored for VRMs. CSCs inherently offer smooth voltage waveforms at the motor terminals, owing to their output filter capacitors, thus mitigating issues such as insulation stress and EMI. Exploiting the unipolar nature of VRM currents, the proposed CSC topology, referred to as *uniCSC*, is simplified to require only a single MOSFET and diode per phase. Furthermore, unlike conventional CSCs, it does not require a dedicated DC link inductor, as the VRM's phase inductance inherently serves this purpose due to the open-end winding configuration. The paper presents the derivation of the topology, explains its modulation method, analyzes the equivalent DC-side parameters, and verifies its operation through transient time-domain simulations.**

***Index Terms*—Variable Reluctance Motor, Switched Reluctance Motor, Current Source Converter, Unipolar Current, Motor Drive, Converter Topology, PWM Modulation**

I. Introduction

Due to their simplicity and robustness, variable reluctance motor (VRM) drive systems present an attractive alternative to induction and permanent magnet motor drives. VRMs produce torque based on the reluctance force generated by the alignment tendency between stator and rotor iron structures, specifically, between stator teeth equipped with wound coils and rotor teeth that carry no windings. Since the reluctance force is proportional to the square of the magnetic flux density in the air gap, the resulting stator coil currents are unipolar, e.g., positive as shown in **Fig. 1**.

The unipolar nature of VRM phase currents enables the use of simplified converter topologies. As a result, numerous converter configurations have been proposed in the literature [1]–[6]. A comprehensive comparison of various converter topologies is presented in [7], where two new converter circuits are introduced, along with a detailed design procedure for the evaluated configurations.

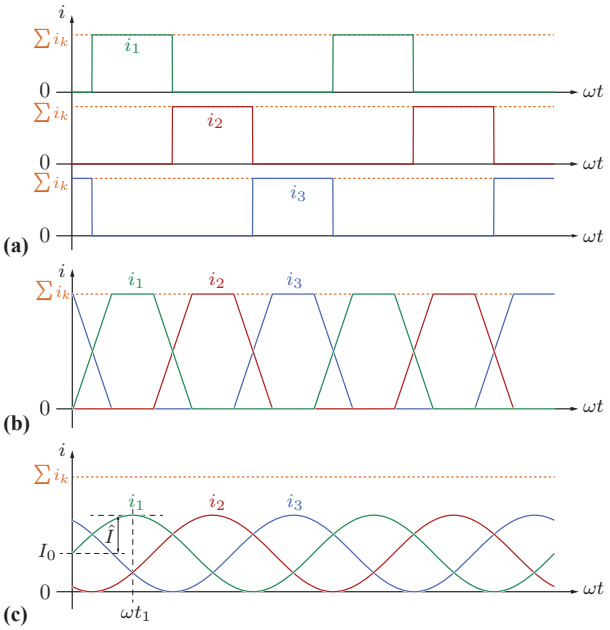

Fig. 1: Three-phase example of unipolar positive currents typically required for supplying VRMs: **(a)** ideally rectangular current pulses, which are challenging to realize in practical VRMs, **(b)** trapezoidal currents with limited $\mathrm{d}i/\mathrm{d}t$, and **(c)** sinusoidal unipolar currents containing both AC and DC components. In all cases, the total current sum across phases, denoted Σi_k, remains constant.

Despite the variety of proposed converter topologies for VRMs, no single standard topology has emerged, unlike the well-established three-phase converter for induction machines and PMSMs, commonly known as the "six-pack." This standard topology has become widely available as an integrated module, benefiting from economies of scale and resulting in highly cost-effective solutions. To leverage the simplicity and affordability of standardized converter hardware, several attempts have been made to adapt existing converter topologies for VRM applications. For example, in [8], a standard three-phase converter is extended with a fourth leg to accommodate the VRM's star point, which is necessary since its unipolar phase currents do not sum to zero. Another approach is presented in [9], where VRM windings are connected in a delta configuration, each phase including a series diode.

More recently, four-leg converter topologies for VRMs have been analyzed [10], where the phases are connected in an open-delta configuration. A similar concept was previously proposed in [5], using an asymmetric converter topology.

A recent wave of research has focused on applying pulse-width modulation (PWM) and vector control techniques to VRMs [11], [12], aiming to simplify their control. Traditional VRM commutation requires precise timing of the switching instants, which becomes increasingly challenging at higher rotational speeds. In contrast, PWM-based approaches offer a more continuous and robust control.

However, the converter topologies employed in these studies are typically based on voltage-source DC links, meaning the VRM windings are subjected to high-frequency pulsed voltages. This can introduce several issues, especially when using wide-bandgap (WBG) semiconductors, which are capable of extremely high $\mathrm{d}v/\mathrm{d}t$ values. Such steep voltage transients can lead to bearing currents, accelerated insulation aging, and increased electromagnetic interference (EMI).

Compared to voltage-source inverters (VSIs) with a DC link, current-source converters (CSCs) offer smoother voltage waveforms across the motor windings, thereby mitigating the aforementioned issues such as bearing currents, insulation stress, and EMI. Motivated by this, the present paper proposes a CSC-based topology for VRMs. Taking advantage of the unipolar nature of VRM phase currents, the proposed CSC topology can be significantly simplified: it requires only one switch and one diode per phase and eliminates the need for a dedicated DC link inductor. Instead, the inherent phase inductance of the VRM fulfills this role. We refer to this topology as the *uniCSC*.

In the following sections, we present the derivation of the uniCSC topology, explain its operating principle and modulation strategy, derive the equivalent DC-side circuit model, and validate its functionality through transient time-domain simulations.

II. Derivation of the uniCSC Topology

As discussed in **Sec. I**, VRMs typically require unipolar phase currents, as illustrated in **Fig. 1**. To enable such current waveforms, this section derives a suitable CSC topology, starting from the classical configuration shown in **Fig. 2(a)**, where L_f denotes the DC link inductance. The DC link current i_dc is typically regulated by an input-stage converter, such as a buck converter supplied from a DC voltage source U_in, as also shown in **Fig. 2(a)**.

As explained in detail in [13], the average value of the phase current, averaged over a switching period, is given by the product of the DC link current and the difference between the upper and lower duty cycles:

$$\langle i_k \rangle = i_\mathrm{dc} \left(d_{\mathrm{u}k} - d_{\mathrm{l}k} \right). \tag{1}$$

Here, the index k denotes the phase number. In the example shown in **Fig. 2(a)**, $k \in \{1, 2, 3\}$, and $d_{\mathrm{u}k}$ and $d_{\mathrm{l}k}$ represent the duty cycles of phase k for the upper and lower CSC cells, respectively.

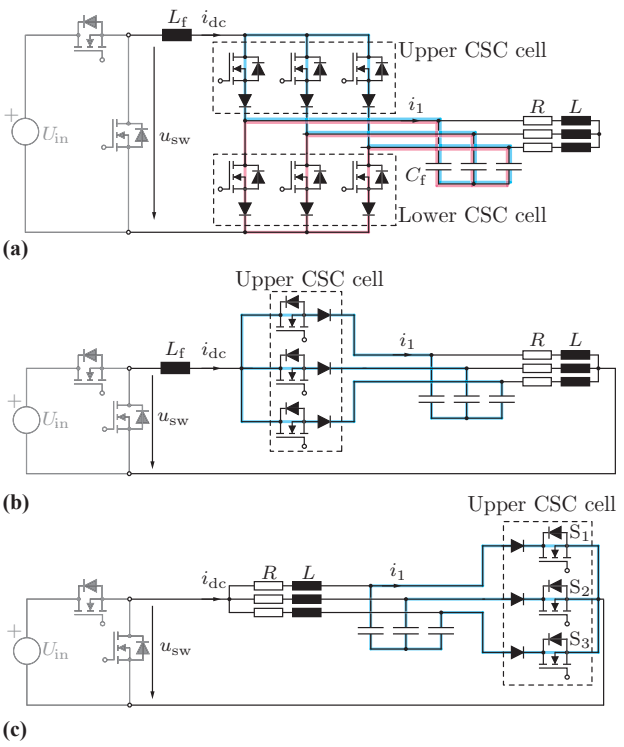

Fig. 2: Derivation of the CSC topology for unipolar currents (uniCSC), starting from: **(a)** a conventional CSI for AC phase currents, composed of two CSC cells, **(b)** a simplified configuration using a single CSC cell to supply unipolar phase currents, and **(c)** the proposed CSC topology, in which the MOSFETs of a CSC cell share a common ground potential and the DC link inductor L_f, typically required in classical CSCs, is omitted.

Equation (1) holds for any average phase current, whether positive or negative. As noted in [13], if the average phase current is positive ($\langle i_k \rangle > 0$), the lower cell's duty cycle can be set to $d_{\mathrm{l}k} = 0$, and the duty cycle of the upper switch is then calculated as $d_{\mathrm{u}k} = \langle i_k \rangle / i_\mathrm{dc}$. Conversely, if the average phase current is negative ($\langle i_k \rangle < 0$), the same logic applies in reverse. To ensure a continuous flow of the DC link current, additional measures such as handling the 'excess duty cycle' must be implemented, as detailed in [13].

Therefore, when a phase current is positive in the CSC topology shown in **Fig. 2(a)**, the corresponding switch in the upper CSC cell actively commutates, while the switch in the lower CSC cell remains off. It is important to note that in a CSC, commutation occurs within each CSC cell, rather than across a half-bridge as in voltage source inverters. Using this analogy, if all phase currents are unipolar, i.e., always positive as shown in **Fig. 1**, only the upper CSC cell is needed to generate the desired phase currents, as illustrated in **Fig. 2(b)**. In this case, the load's star point must be connected to the DC minus rail, since the unipolar phase currents do not sum to zero. Instead, their sum is equal to the DC link current: $\sum i_k = i_1 + i_2 + i_3 = i_\mathrm{dc}$.

The converter topology shown in **Fig. 2(b)** employs

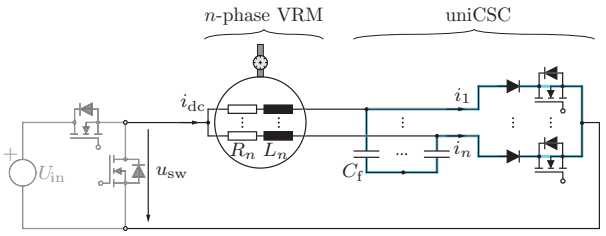

Fig. 3: Proposed uniCSC with arbitrary number of phases n.

a single CSC cell to commutate unipolar positive phase currents. As a result, only one switch (MOSFET) and one diode per phase are required. Similar to the conventional CSC topology in **Fig. 2(a)**, the DC link current i_{dc} is commutated within the CSC cell, this also applies to the simplified single-cell converter in **Fig. 2(b)**. As mentioned in the **Sec. I**, we refer to this simplified converter as uniCSC, indicating a CSC for unipolar currents.

In the conventional CSC, the DC link current is impressed using a dedicated DC link inductor L_{f}, which is initially retained in the derivation of the uniCSC topology in **Fig. 2(b)**. However, since the uniCSC is intended to supply VRMs, an inherently inductive load where each phase includes inductance, these phase inductances effectively reflect into the DC link circuit and act as an equivalent series inductance. Therefore, the external inductor L_{f} can be omitted without loss of functionality, resulting in the simplified circuit shown in **Fig. 2(c)**.

Additionally, in the final uniCSC topology of **Fig. 2(c)**, the MOSFETs and diodes are rearranged such that the MOSFET source terminals connect directly to the DC minus rail. This enables the use of non-isolated gate drivers, further simplifying hardware design. As a result, the uniCSC becomes more cost-effective and component-efficient.

The proposed uniCSC topology can be extended to a VRM with an arbitrary number of phases n, as illustrated in **Fig. 3**. In this general case, the uniCSC requires n MOSFETs and n diodes, one of each per phase. Additionally, a minimum of two MOSFETs or one MOSFET and one diode is needed for the input converter to regulate the DC link current when a half-bridge configuration is used.

III. uniCSC Operation Principle

In contrast to the conventional CSC, where the average phase current is determined by the product of the DC link current and the difference between the upper and lower CSC cells' duty cycles, as expressed in (1), the proposed uniCSC employs only a single CSC cell. Consequently, the average phase current is given by

$$\langle i_k \rangle = d_k i_{\mathrm{dc}}, \tag{2}$$

where d_k is the duty cycle, defined as the relative time duration for which MOSFET S_k is turned on, k denotes the phase index, and $\langle \cdot \rangle$ denotes average value over the switching period. Therefore, the duty cycles for the uniCSC can be directly computed from the desired average phase currents and the DC link current as

$$d_k = \frac{\langle i_k \rangle}{i_{\mathrm{dc}}}. \tag{3}$$

As with any CSC cell, the uniCSC must ensure a continuous conduction path for the DC link current at all times. This means that there must never be an instant when all MOSFETs are turned off. Consequently, each CSC cell, uniCSC included, must always have exactly one MOSFET conducting at any given time. This imposes a constraint on the conduction durations $d_k T_{\mathrm{sw}}$ of each MOSFET, where T_{sw} is the switching period. Specifically, the sum of all conduction intervals must equal one full switching period, which leads to the condition on the duty cycles:

$$d_{\mathrm{tot}} = \sum_{k=1}^{n} d_k = 1. \tag{4}$$

To explain better modulation process of the uniCSC, an example is considered where the time moment ωt_1 denoted in **Fig. 1(c)** is zoomed in to the level of a single switch period. The current waveforms in **Fig. 1(c)** can be expressed as

$$\begin{aligned} \langle i_1 \rangle &= \hat{I} \sin(\omega t + \theta_i) + I_0 \\ \langle i_2 \rangle &= \hat{I} \sin(\omega t + \theta_i - \frac{2\pi}{3}) + I_0, \\ \langle i_3 \rangle &= \hat{I} \sin(\omega t + \theta_i - \frac{4\pi}{3}) + I_0 \end{aligned} \tag{5}$$

where $\hat{I}$ is the peak value of the AC component, I_0 is the DC component of the current, ω is the electrical angular frequency, and θ_i is the initial current angle. For the waveforms depicted in **Fig. 1(c)**, $\theta_i = -\pi/2$, $I_0 = i_{\mathrm{dc}}/3$, and $\hat{I} = I_0 = i_{\mathrm{dc}}/3$. Therefore, for the considered time moment ωt_1, the averaged phase currents are equal to

$$\langle i_1 \rangle = \frac{2 i_{\mathrm{dc}}}{3}, \quad \langle i_2 \rangle = \langle i_3 \rangle = \frac{i_{\mathrm{dc}}}{6}. \tag{6}$$

Using (3), the duty cycles at the specific time instant ωt_1 are calculated as

$$d_1 = \frac{2}{3}, \quad d_2 = \frac{1}{6}, \quad \text{and} \quad d_3 = \frac{1}{6}. \tag{7}$$

As previously discussed, to ensure a continuous conduction path for the DC link current, the duty cycles satisfy the condition $d_1 + d_2 + d_3 = 1$. Based on these duty cycles, the corresponding gate signals for controlling the switches are generated using a multiple-threshold modulator (cf. [13]), as illustrated in **Fig. 4(a)**. This PWM technique ensures that gate signals are sequentially activated, similar to a relay race, with no overlap in conduction. At any given moment, exactly one switch is conducting, and the total conduction time over a switching period sums up to T_{sw}, as can be seen in **Fig. 4(b)** for the resulting gate signal pulses.

The resulting phase currents i_1, i_2, and i_3 are pulsed waveforms, as illustrated in **Fig. 4(c)**, with pulse amplitudes equal to the DC link current i_{dc}. The corresponding circuit configurations for each conduction state, i.e., all

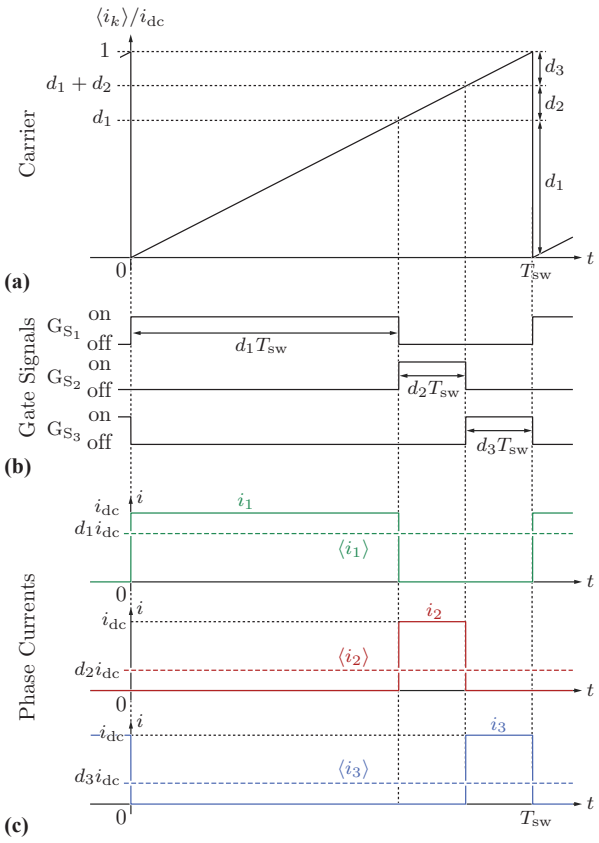

Fig. 4: Modulation of the uniCSC: **(a)** multiple-threshold pulse-width modulation principle, **(b)** resulting gate signals, and **(c)** corresponding phase currents.

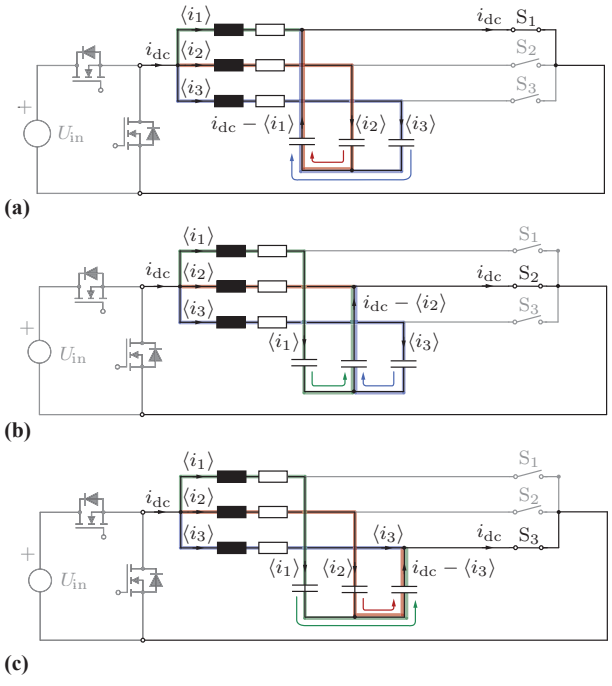

Fig. 5: Switching states of the three-phase uniCSC: **(a)** phase 1 conducts the DC link current, **(b)** phase 2 conducts the DC link current, and **(c)** phase 3 conducts the DC link current. For each state, the corresponding capacitor currents are indicated. These three states represent the only valid switching configurations for the uniCSC.

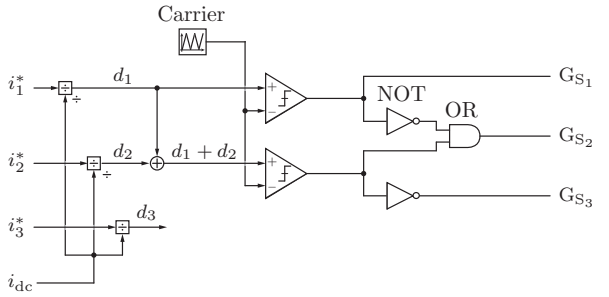

Fig. 6: Block diagram of the uniCSC modulation scheme, illustrating the signal flow from phase current references to gate signal generation.

valid switching states, are shown in **Fig. 5**. No other switching combinations are permitted. These pulsed currents are filtered by the output capacitors C_f, yielding average currents delivered to the VRM. Consequently, the VRM phase currents correspond to the average values of the pulsed currents and are given by $\langle i_1 \rangle = d_1 i_\mathrm{dc}$, $\langle i_2 \rangle = d_2 i_\mathrm{dc}$, and $\langle i_3 \rangle = d_3 i_\mathrm{dc}$. These average currents are regulated by controlling the pulse widths, that is, the conduction durations of the respective switches, according to the desired phase current references i_1^*, i_2^*, and i_3^*.

The implementation of the multiple-threshold modulator to obtain the desired phase currents load is shown in **Fig. 6**. Notably, this realization inherently guarantees a continuous current path for the DC link current without explicitly requiring the value of the last duty cycle d_3. Instead, it is automatically enforced as $d_3 = 1 - d_1 - d_2$.

For an n-phase system, the final duty cycle is similarly determined by

$$d_n = 1 - \sum_{k=1}^{n-1} d_k, \tag{8}$$

as discussed in [13]. The extension of the multiple-threshold modulator to n phases is straightforward: it involves replicating the comparator and digital logic blocks used for the three-phase case in **Fig. 6**; see also [13].

IV. Equivalent DC-Side Parameters

The previous section explained the operation of the proposed uniCSC, detailing its modulation strategy and the commutation of the DC link current among the phases. The DC link current itself is regulated by an input converter, which effectively ”sees” the uniCSC and its load (i.e., the VRM) as an equivalent DC load. Therefore, the objective of this section is to derive the equivalent DC-side parameters of the uniCSC. To focus on the converter operation, a pure RL load is assumed in this section, as shown in **Fig. 7(a)**.

We consider sinusoidal unipolar current waveforms, as exemplified for the three-phase case in **Fig. 1(c)**. Regardless of the number of phases or the specific waveform shape, the instantaneous sum of all phase currents must equal the DC link current:

$$\sum_{k=1}^{n} i_k = i_\mathrm{dc}. \tag{9}$$

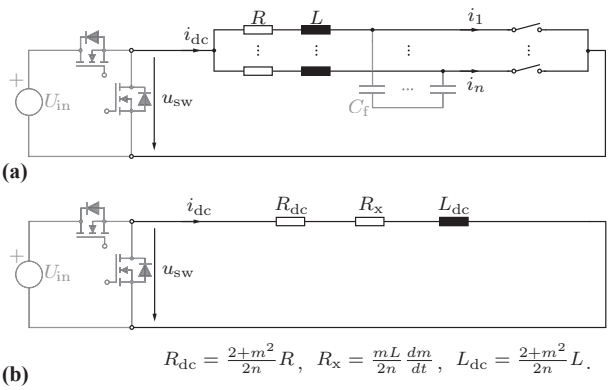

Fig. 7: Derivation of the equivalent DC-side circuit model: **(a)** schematic of a general n-phase uniCSC supplying an RL load with back-EMF, and **(b)** resulting equivalent DC-side circuit model.

Parameter	Symbol	Value
Sinusoidal Operation		
Input current	i_{dc}	40 A
Output capacitance	C_{f}	4.7 µF
Load resistance	R	1 Ω
Load inductance	L	3.5 mH
Switching frequency	f_{sw}	200 kHz
Fundamental frequency	$f_0 = 1/T_0$	50 Hz

TABLE I: Simulation Parameters.

Since the AC components of the sinusoidal waveforms always sum to zero, this condition implies that the DC component of each phase current must be $I_0 = i_{\mathrm{dc}}/n$.

The peak value of the AC component, denoted $\hat{I}$, cannot exceed I_0. To generalize this, a modulation index $m \in [0, 1]$ is introduced, defining the AC peak as $\hat{I} = m\, i_{\mathrm{dc}}/n$. Consequently, the expression for the average phase current becomes:

$$\langle i_k \rangle = m\frac{i_{\mathrm{dc}}}{n}\cos\left(\omega t + \theta_i - (k-1)\frac{2\pi}{n}\right) + \frac{i_{\mathrm{dc}}}{n}, \quad (10)$$

where $k \in \{1, \ldots, n\}$ denotes the phase index.

The derivation of the equivalent DC-side parameters is based on power balance averaged over the switching period, where we assume that the input DC power must equal the sum of the powers delivered to each phase, see **Fig. 7(a)**:

$$\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} = \sum_{k=1}^{n} \langle u_k \rangle \langle i_k \rangle, \quad (11)$$

where $\langle u_{\mathrm{sw}} \rangle$ denotes the average value of the pulsed DC link voltage. The voltage of each phase is modeled as

$$\langle u_k \rangle = R\langle i_k \rangle + L\frac{\mathrm{d}\langle i_k \rangle}{\mathrm{d}t}, \quad (12)$$

with R and L representing the phase resistance and inductance, respectively.

It should be noted that the effect of the filter capacitors C_{f} is neglected in the power balance equation (11), as these capacitors primarily filter high-frequency current components and have a negligible impact at the fundamental frequency range, where the power balance is evaluated.

If we assume that the voltage drop in (12) is solely due to the phase resistance, the power balance equation (11) simplifies to

$$\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} = \sum_{k=1}^{n} R\langle i_k \rangle^2. \quad (13)$$

Substituting the expression for the phase currents from (10) into this equation and performing the summation yields

$$\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} = \underbrace{\frac{2+m^2}{2n} R}_{=R_{\mathrm{dc}}}\, i_{\mathrm{dc}}^2, \quad (14)$$

from which the equivalent DC-side resistance can be identified as $R_{\mathrm{dc}} = \frac{2+m^2}{2n} R$. It is important to note that the equivalent DC-side resistance R_{dc} depends on the modulation index m. Its minimum value occurs at $m = 0$, yielding $R_{\mathrm{dc}} = R/n$, which corresponds to the expected result for n parallel-connected phase resistances of value R.

If we now assume that the voltage drop in (12) is solely due to the phase inductance, the power balance equation (11) becomes

$$\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} = \sum_{k=1}^{n} L\frac{\mathrm{d}\langle i_k \rangle}{\mathrm{d}t}\, \langle i_k \rangle, \quad (15)$$

where L is the inductance of each phase. Substituting the expression for the phase current from (10) into this equation yields

$$\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} = \underbrace{\frac{mL}{2n}\frac{\mathrm{d}m}{\mathrm{d}t}}_{=R_{\mathrm{x}}}\, i_{\mathrm{dc}}^2 + \underbrace{\frac{2+m^2}{2n} L}_{=L_{\mathrm{dc}}}\, \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t}\, i_{\mathrm{dc}}, \quad (16)$$

where the phase inductance L results in two equivalent effects on the DC side: a dynamic resistance term R_{x}, which accounts for the power increase or decrease due to variations in the modulation index m (see [14]), and an equivalent DC-side inductance L_{dc}.

Similar to the equivalent resistance R_{dc}, the minimum value of the equivalent DC-side inductance is $L_{\mathrm{dc}} = L/n$, which occurs when the modulation index $m = 0$. This represents the lowest inductance required to sustain continuous DC link current operation in the uniCSC. As a result, the presence of this equivalent inductance, arising from the phase inductances themselves, eliminates the need for a dedicated external DC link inductor in the proposed uniCSC topology, see **Fig. 2**.

The resulting equivalent DC-side circuit, along with the summarized expressions for its parameters, is shown in **Fig. 7(b)**.

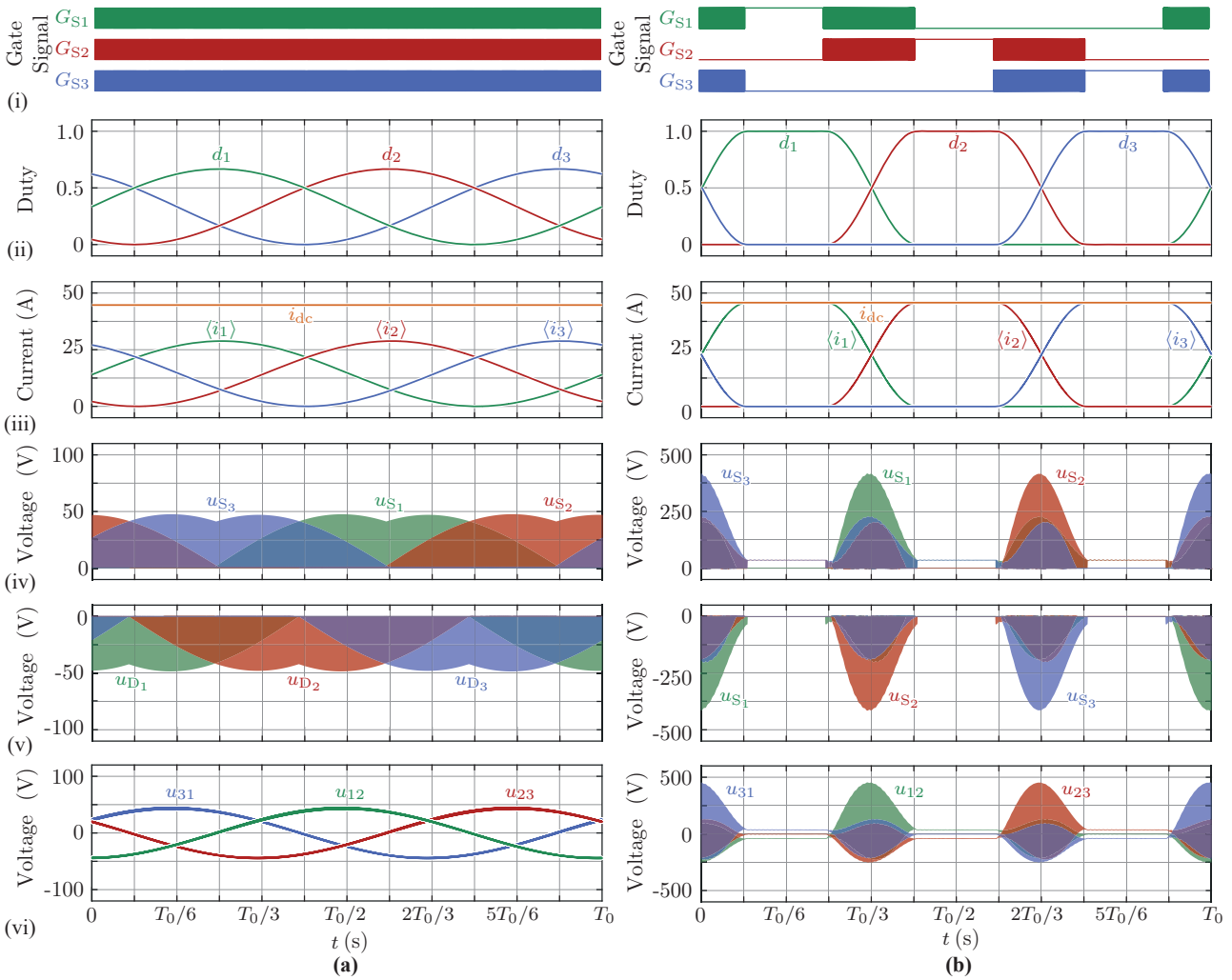

Fig. 8: Simulation waveforms for **(a)** sinusoidal reference and **(b)** trapezoidal reference. From top to bottom; **(i)** gate signals of switching devices, **(ii)** duty cycles, **(iii)** dc and phase currents, **(iv)** switching device voltages, **(v)** diode voltages, **(vi)** line-to-line capacitor voltages.

V. Simulation Results

Time-domain simulations are conducted to validate the operational principles of the proposed uniCSC, using an R-L load with parameters summarized in **Tab. I**. A complementary analysis, including simulations with a VRM, is provided in [15], where the advantages of the uniCSC-fed VRM are highlighted, particularly in simplifying control and achieving behavior similar to that of a series-excited DC machine.

In the sinusoidal operation shown in **Fig. 8(a)**, the phase current closely follows the explicitly defined duty cycle (see **Fig. 8(a.ii) and (a.iii)**), confirming the intended current-source converter behavior without DC-link inductor. For each switching device, the maximum positive line-to-line voltage connected to the device, e.g. $\max(u_{12}, u_{23}, u_{31})$ for S_1, is applied, while the corresponding diodes block the negative voltage in the reverse direction, as illustrated in **Fig. 8(a.iv) and (a.v)**. The line-to-line voltages across the output capacitors are determined by the load impedance, as the phase currents are impressed, see equivalent circuit depicted in **Fig. 5**.

Fig. 8(b) illustrates the simulation waveforms obtained under trapezoidal current reference operation. To mitigate voltage spikes caused by steep $\mathrm{d}i/\mathrm{d}t$ transients, the rising and falling edges of the trapezoidal current waveform are smoothed using cosine interpolation.

As in the sinusoidal case, the phase currents closely follow the duty cycle references due to the current-source behavior of the converter, as shown in **Fig. 8(b.ii)** and **(b.iii)**. However, elevated line-to-line voltages are observed during current transitions between phases, see **Fig. 8(b.iv)–(b.vi)**. This behavior is expected, as these voltages are responsible for driving the current transitions.

For example, when the current $\langle i_1 \rangle$ decreases from its peak value i_{dc} to zero, and $\langle i_2 \rangle$ simultaneously increases, the current is effectively "handed over" from phase 1 to phase 2. This transition is driven by the line-to-line voltage u_{12}, which becomes high and positive during this interval. A faster transition—i.e., a higher $\mathrm{d}i/\mathrm{d}t$—would result in an even larger u_{12}. Thus, in the uniCSC topology, the speed of current transitions is fundamentally limited

by both the blocking voltage capability of the devices and the passive parameters of the motor phases. Similar observations apply to other transitions: u_{23} becomes high when $\langle i_2 \rangle$ decreases and $\langle i_3 \rangle$ increases, while u_{31} rises during the transition from phase 3 back to phase 1. A detailed analysis of these transition dynamics is beyond the scope of this paper and is reserved for future work.

These results demonstrate that the uniCSC is capable of handling unipolar current waveforms with overlap, such as sinusoidal currents where multiple phases conduct simultaneously, not only during current transitions. This capability is particularly important for VRM converters, as many topologies are unable to accommodate overlapping phase currents. Additionally, the simulations confirm that the uniCSC can effectively support trapezoidal current waveforms as well.

VI. Conclusions

This paper has proposed a current source converter (CSC) topology specifically tailored for variable reluctance motors (VRMs). Compared to voltage source inverters (VSIs), CSCs offer smoother voltage waveforms across the motor windings, which is advantageous for mitigating electromagnetic interference and insulation stress. In the case of VRMs, which inherently require unipolar phase currents, the CSC topology can be significantly simplified: only one MOSFET and one diode are needed per phase. We refer to this simplified topology as *uniCSC*, highlighting its suitability for unipolar current drive applications.

A key advantage of the uniCSC is that, unlike conventional CSCs, it does not require a dedicated DC link inductor. This is enabled by the open-end winding configuration of VRMs and the presence of a DC current component, which allows the motor's own inductance to fulfill this role. We derived the uniCSC topology starting from the conventional CSC structure, explained the associated modulation scheme, and analyzed its equivalent behavior from the DC-side perspective. The proposed operation was validated through time-domain simulations using both sinusoidal and trapezoidal unipolar phase current waveforms.

Future work will focus on the hardware implementation of the uniCSC and the development of a VRM test bench, where the proposed drive system will be experimentally validated under various operating conditions.

Appendix A
Equivalent Model of uniCSI

This appendix derives the equivalent DC-side parameters for a Variable Reluctance Machine (VRM). In this analysis, the machine is modeled as a switched reluctance machine (SRM), wherein the mutual inductances between phases are negligible due to the magnetic and physical isolation of each phase winding. This assumption is consistent with conventional SRM modeling practices, where each phase operates independently and the magnetic coupling between phases is minimized by design.

In addition to the phase currents defined in (10), the self-inductance of each phase is modeled by its fundamental component as

$$L_k = \frac{L_\Sigma}{2} + \frac{L_\Delta}{2} \cos\left(\omega t + (k-1)\frac{2\pi}{n}\right), \tag{17}$$

where L_Σ and L_Δ represent the sum and difference of the aligned and unaligned inductances, respectively. This expression represents the dominant harmonic of the inductance variation, and higher-order spatial harmonics are neglected for analytical simplicity. This formulation reflects the periodic variation of inductance with respect to the electrical angle ωt. Throughout this analysis, the number of phases n is assumed to be greater than 3.

The voltage drop across each phase consists of a resistive component Ri_k and the contribution from the time-varying flux linkage. Following the power balance formulation introduced in (11), the total DC-side input power is expressed as

$$\begin{aligned}\langle u_{\mathrm{sw}} \rangle i_{\mathrm{dc}} &= \sum_{k=1}^{n} \left(R i_k^2 + \frac{dL_k}{dt} i_k^2 + L_k \frac{di_k}{dt} i_k \right) \\ &= R_{\mathrm{dc}} i_{\mathrm{dc}}^2 + L_{\mathrm{dc}} \frac{di_{\mathrm{dc}}}{dt} i_{\mathrm{dc}} + R_{\mathrm{x}} i_{\mathrm{dc}}^2 + R_\tau i_{\mathrm{dc}}^2.\end{aligned} \tag{18}$$

Each term on the right-hand side represents an equivalent DC parameter:

- R_{dc}: equivalent resistance due to copper losses in the stator windings,
- L_{dc}: equivalent inductance representing average magnetic energy storage,
- R_{x}: apparent resistance associated with modulation index variation, and
- R_τ: equivalent resistance representing mechanical power output.

These parameters are given from (18) by

$$R_{\mathrm{dc}} = \frac{2+m^2}{2n} R, \tag{19}$$

$$L_{\mathrm{dc}} = \frac{(2+m^2)L_\Sigma + 2m\cos(\theta_i) L_\Delta}{4n}, \tag{20}$$

$$R_{\mathrm{x}} = \frac{mL_\Sigma + \cos(\theta_i) L_\Delta}{4n} \frac{dm}{dt}, \tag{21}$$

$$R_\tau = \frac{m\omega \sin(\theta_i) L_\Delta}{4n}. \tag{22}$$

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