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Performance review of state-of-the-art 1.2 kV SiC devices based on experimental figures-of-merit

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Abstract Power electronic systems, such as photovoltaic inverters and drive systems, increasingly use wide bandgap semiconductors like Gallium Nitride and Silicon Carbide (SiC). With SiC devices widely available, many are packaged in TO-247-4 and offer comparable on-state resistances and blocking voltages. However, supply shortages raise the question of whether devices from different manufacturers can be interchanged without design changes. This paper analyzes SiC devices from multiple manufacturers using empirical measurements in a bridge-leg configuration at voltages up to 950 V and temperatures up to 150 °C. Charge independence over junction temperature is quantified, and measurement-based Figures of Merit (FOMs) are compared. Results show similar performance in hard-switched converters with minimal overlap losses. However, in soft-switching applications, the first device achieves 1.5 times better FOM, while in high-current scenarios with significant overlap losses, the third device excels with a FOM nearly three times higher. These findings are further validated by *dv/dt* measurements.

Keywords Silicon carbide (SiC) devices · 1.2 kV power devices · Measurement-based figures-of-merit · High-temperature

Leistungsbewertung modernster 1,2-kV-SiC-Bauelemente basierend auf experimentellen Figures-of-Merit

Zusammenfassung Leistungselektronische Systeme wie Photovoltaik-Wechselrichter und Antriebssysteme setzen zunehmend auf Wide Bandgap-Halbleiter wie Galliumnitrid und Siliziumkarbid (SiC). Mit der breiten Verfügbarkeit von SiC-Bauelementen sind viele in TO-247-4-Gehäusen erhältlich und bieten vergleichbare Durchlasswiderstände sowie Sperrspannungen. Allerdings werfen Lieferengpässe die Frage auf, ob Bauelemente verschiedener Hersteller ohne Designanpassungen austauschbar sind. Diese Arbeit analysiert SiC-Bauelemente mehrerer Hersteller anhand empirischer Messungen in einer Halbbrückenkonfiguration bei Spannungen bis zu 950 V und Temperaturen bis zu 150 °C. Die Ladungsunabhängigkeit über die Sperrschichttemperatur wird quantifiziert, und messbasierte Figures of Merit (FOMs) werden verglichen. Die Ergebnisse zeigen eine ähnliche Leistung in hart geschalteten Wandlern mit minimalen Überlappungsverlusten. In weich schaltenden Anwendungen erreicht jedoch das erste Bauelement einen 1,5-fach besseren FOM, während das dritte Bauelement in Hochstromszenarien mit erheblichen Überlappungsverlusten durch einen nahezu dreifach höheren FOM herausragt. Diese Erkenntnisse werden durch dv/dt-Messungen weiter validiert.

Schlüsselwörter Siliciumkarbid (SiC)-Bauelemente · 1,2-kV-Leistungsbauelemente · Messbasierte Gütemaße · Hochtemperatur

1 Introduction

Modern switched-mode power electronic converter systems increasingly incorporate wide bandgap (WBG) power semiconductors to augment the efficiency of power conversion processes. Gallium Nitride (GaN) and Silicon Carbide (SiC) are the prominent WBG semiconductor materials used in state-of-the-art power converter systems. GaN is favored for 450 V [1] DC-link voltage applications, while SiC is the ma-

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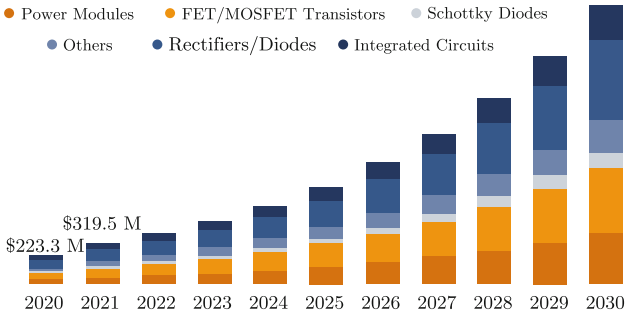

Fig. 1 The projected growth of the U.S. SiC semiconductor devices market from 2020 to 2030, measured in U.S. dollars (millions). The forecast suggests a diverse expansion across all categories, reflecting the increasing adoption of SiC devices in various applications, see [25]

terial favored for power electronic systems operating at voltages above 500 V [2].

The exceptional performance attributes of SiC [3, 4], facilitate the realization of power electronic converter systems with enhanced efficiency and increased power density, making them particularly advantageous for grid-tied systems or those supplied by high-voltage batteries [5, 6]. Typical examples of such applications range between several kilo-watts up to several tens of kilo-watts, such as photovoltaic (PV) inverters [7, 8], power factor correction (PFC) rectifier systems in the telecommunication sector for supplying, e.g., data centers [9, 10], advanced industrial drive systems [11, 12], integrated (onboard) chargers for electric vehicles (EVs) [13–15], and EV propulsion systems [16], to mention a few.

Adopting WBG devices in a specific application can be economically justified by their lower loss characteristics compared to silicon devices [17]. For instance, integrating SiC devices within the inverter of an EV motor drive system significantly influences the entire powertrain. This is primarily because their reduced losses lead to lower heat generation, enabling a downsizing of the cooling system. Such a reduction decreases the EV's overall weight and facilitates an extended driving range. Alternatively, if the desired range is maintained, it allows for a smaller battery pack. Ultimately, this cascades into a tangible reduction in the vehicle's weight and the costs associated with cooling and battery systems. This cost-efficiency can offset the initial higher investment in SiC devices, making them a financially viable option in the long term [18, 19].

In light of the projected surge in demand for EVs, grid storage systems, and PV inverters [20–24], SiC devices are predicted to have exponential market growth, as illustrated in Fig. 1. This growing demand presents a substantial business opportunity, prompting an increasing number of manufacturers to enter the SiC power semiconductor market. Consequently, the market's expansion has underscored the necessity for rigorous characterization and comparison of devices from various manufacturers. Such analyses are vital for power electronics engineers, simplifying the decision-making process in selecting appropriate devices for their projects. Determining whether performance differences exist among SiC devices from different manufacturers is crucial, as identifying uniformity in performance would facilitate second sourcing without additional design complexities. Conversely, if variances are present, it becomes imperative to quantify these differences and evaluate their impact on converter performance.

For the comparison of the devices, we use Figure of Merit (FOM) listed in Tab. 1, which were initially introduced for evaluating the material properties essential to the functionality of devices, encompassing critical electric field, electron mobility, and thermal conductivity [26–29]. Semiconductor device development aims to improve the trade-off relationship among on-resistance, parasitic capacitances, breakdown voltage, and short-circuit withstand time [30]. For 1.2 kV SiC devices, optimization studies of cell layout, JFET regions, and P-well regions have been conducted using FOMs as performance indicators [31–33].

These foundational FOMs, when integrated with advancements in manufacturing processes and packaging techniques, evolved into what we refer to as die-area-independent device FOMs. Such FOMs encapsulate higher-level device parameters, including on-state resistance $R_{ds,on}$, output charge Q_{oss}, gate charge Q_g or Miller charge Q_M, providing a comprehensive framework for comparison across different technologies, manufacturers, or breakdown voltages. To ensure a fair comparison of devices from different manufacturers, relying on FOMs derived from experimentally obtained data rather than datasheet specifications is essential. This approach mitigates the potential bias wherein manufacturers may present their devices in an overly favorable light, which might not reflect their actual performance in practical applications. Thus, in this paper, we estimate the FOMs based on measured data, which offer a genuine perspective on the device's performance, enabling a more accurate and reliable assessment. It should be noted that this method is not officially certified or licensed, but similar approaches are being used for device characterization [37, 38], and the used equipments are certified.

Tab. 1 FOMs from literature linked to power dissipation characteristics of the switching devices

Name/Symbol	Analytic Expression	Based on Literature References
FOM_I	$\frac{1}{R_{ds,on}Q_{oss}}$	[34]
FOM_{II}	$\frac{1}{R_{ds,on}Q_{g0}}$	[35]
FOM_{III}	$\frac{1}{R_{ds,on}Q_M}$	[36]

2 Experimental setup

This section introduces the hardware demonstrator and the employed high-temperature measurement

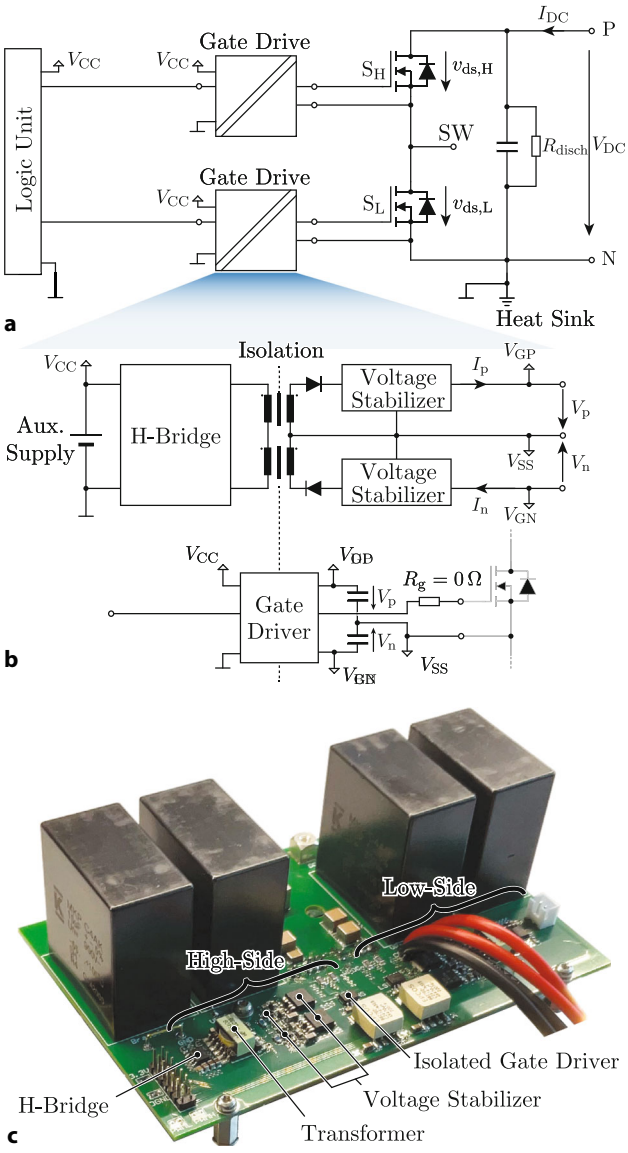

Fig. 2 (**a**) Schematic of the hardware demonstrators designed to evaluate the Figure of Merit (FOM) of considered power semiconductors S_H and S_L. (**b**) Schematic of the gate drive circuit, including the voltage stabilizers, to ensure constant gate drive voltage levels of $V_p = 15\,V$ and $V_n = -3.8\,V$ across characterization. Indicated terminals are used to measure the gate drive voltages and currents. (**c**) Hardware demonstrator of the assembled half-bridge

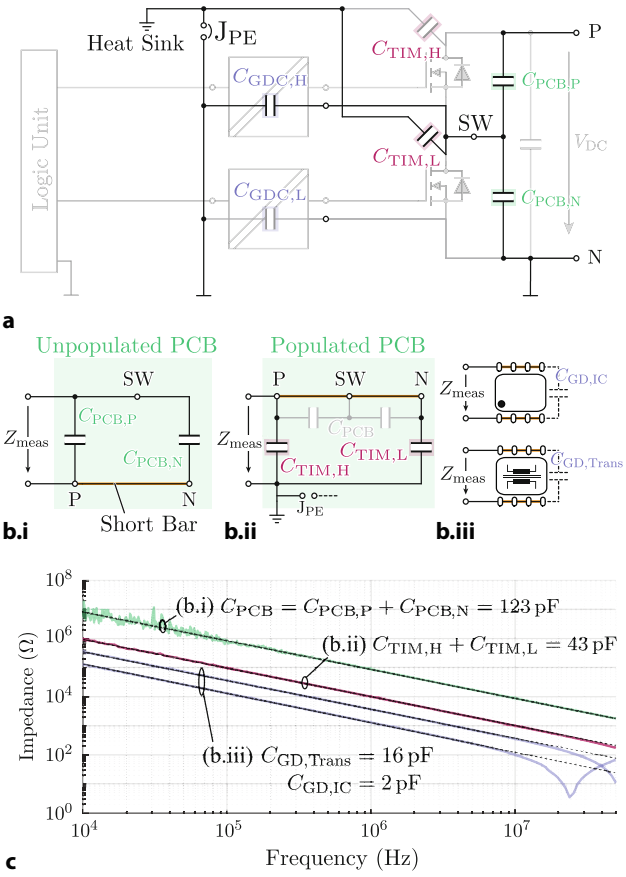

Fig. 3 (**a**) Schematic highlighting contributions to the parasitic switch-node capacitance C_{par} in the employed hardware demonstrator. $C_{PCB,P}$ and $C_{PCB,N}$ denote the parasitically formed capacitances between PCB tracks, $C_{TIM,H}$ and $C_{TIM,L}$ the drain tab of high- and low-side switching devices to heat sink capacitance, and $C_{GDC,H}$ and $C_{GDC,L}$ the parasitic capacitances introduced by the gate drive circuit for high- and low-side switching devices. (**b**) Equivalent circuits for various impedance measurements to determine the parasitic capacitances. (**c**) Impedance measurement results that are used to deduce the values of the parasitic capacitances in (1)

setup to characterize the FOMs of the device-under-test (DUT).

2.1 Half-bridge hardware demonstrator

The details of the designed hardware demonstrator rated for a DC-link voltage up to 950 V and an ambient temperature of up to 150 °C are shown in Fig. 2. The demonstrator is designed to employ two TO-247-4 power transistors (S_H and S_L, cf. Fig. 2a) positioned close to each other to minimize the commutation loop and securely mounted onto a heatsink using a thermal interface material (TIM) that ensures effective thermal conduction and provides the necessary electrical insulation.

The identical layout of the isolated gate drive circuits ensures equivalent performance for low- and high-side power transistors. The gate resistor was chosen with $R_g = 0\,\Omega$ to benchmark the limit of the device, i.e., maximum dv/dt values [12]. However, it should be noted that the measured on-state resistance, gate charge, and output charge are independent of the gate resistor. Furthermore, in industrial applications typically employ a non-zero gate resistor [39, 40]. The gate driver IC [41] operates at a positive gate voltage of $V_p = +15\,V$ for turn on and a negative gate voltage $V_n = -3.8\,V$ for turn off, ensuring to stay within the safe-operating-area (SOA) for all evaluated MOSFETs. Stable gate drive voltages are ensured by a voltage stabilizer, containing a voltage tracker [42] with its output voltages referenced by a low dropout (LDO) voltage

regulator, within the positive and negative supply rail as shown in Fig. 2b. This approach is essential to operate the DUT at consistent voltage levels across varying switching frequencies, i.e., varying gate driver power demands. With a specified power of 3 W, the gate drive circuit can handle the power transistors at switching frequencies as high as $f_{sw} = 1\,\text{MHz}$. This high f_{sw} capability is crucial for accurately measuring the output charge Q_{oss} at lower DC-link voltages.

The assembled hardware demonstrator is shown in Fig. 2c, indicating terminals within the low-side gate drive circuit used to measure the gate drive DC voltages V_p, V_n and gate drive DC currents I_p, I_n (cf. Fig. 2b). These quantities allow the derivation of the gate drive power within operation, as needed to characterize the gate charge Q_g and later to obtain the Miller charge Q_M.

To characterize the output charge Q_{oss} by zero-current switching (ZCS) experiments, it is crucial to quantify the parasitic switch-node capacitance C_{par} arising from the actual construction of the hardware demonstrator. The total (parasitic) switch-node capacitance C_{par} includes the capacitance C_{PCB} resulting from the PCB layout, the capacitance formed between the heat sink and the drain pad insulated by TIM $C_{TIM} = C_{TIM,H} = C_{TIM,L}$ and the capacitance associated with the gate drive circuit $C_{GDC} = C_{GDC,H} = C_{GDC,L}$ as also shown in Fig. 3a.

$C_{PCB,P}$ and $C_{PCB,N}$ are identified as the capacitance between the switch-node SW and the DC bus, represented by either the positive or the negative DC-link rail P or N. To measure C_{PCB}, one must short the DC-link rails on the PCB when no components are present, which equivalently results in total $C_{PCB} = C_{PCB,P} + C_{PCB,N}$ that will be seen in the measurement, see Fig. 3b.i. Using an impedance analyzer on the switch-node SW and the shorted P-N terminal, we can deduce from the impedance measurement that $C_{PCB} = 123\,\text{pF}$, see Fig. 3c. Furthermore, $C_{TIM,H}$ and $C_{TIM,L}$, established by the TIM employed on high- and low-side switching devices, can be measured by shorting the DC-link rails to the switch node on a component-populated PCB mounted on the heatsink. Ensuring the heatsink's protective earth (PE) jumper is open, see Fig. 3b.ii, the measured capacitance between P-N-SW and heatsink measures $C_{TIM,H} + C_{TIM,L} = 43\,\text{pF}$, see Fig. 3c. Due to symmetry, we assume TIM capacitances are equal, resulting in $C_{TIM,H} = C_{TIM,L} = 21.5\,\text{pF}$. The isolation requirement of the gate drive components, specifically the gate driver IC and the transformer, cause $C_{GDC} = C_{GDC,Trans} + C_{GDC,IC}$. When measured separately with an impedance analyzer, see Fig. 3b.iii, the gate driver IC accounts for 2 pF, and the transformer contributes 16 pF, see Fig. 3c. Thus, the total gate drive capacitance is $C_{GDC} = 18\,\text{pF}$. In summary, the total parasitic switch-node capacitance of the half-bridge leg, C_{par}, is the sum of the PCB capacitance, one TIM capacitance, and one gate drive capacitance, yielding

$$C_{par} = C_{PCB} + C_{TIM,L} + C_{GDC,H} = 162.5\,\text{pF}. \quad (1)$$

It should be noted that $C_{TIM,H}$ and $C_{GDC,L}$ do not affect the switch-node parasitic capacitance C_{par}, as the heatsink and the logic ground are connected to the negative DC-link rail.

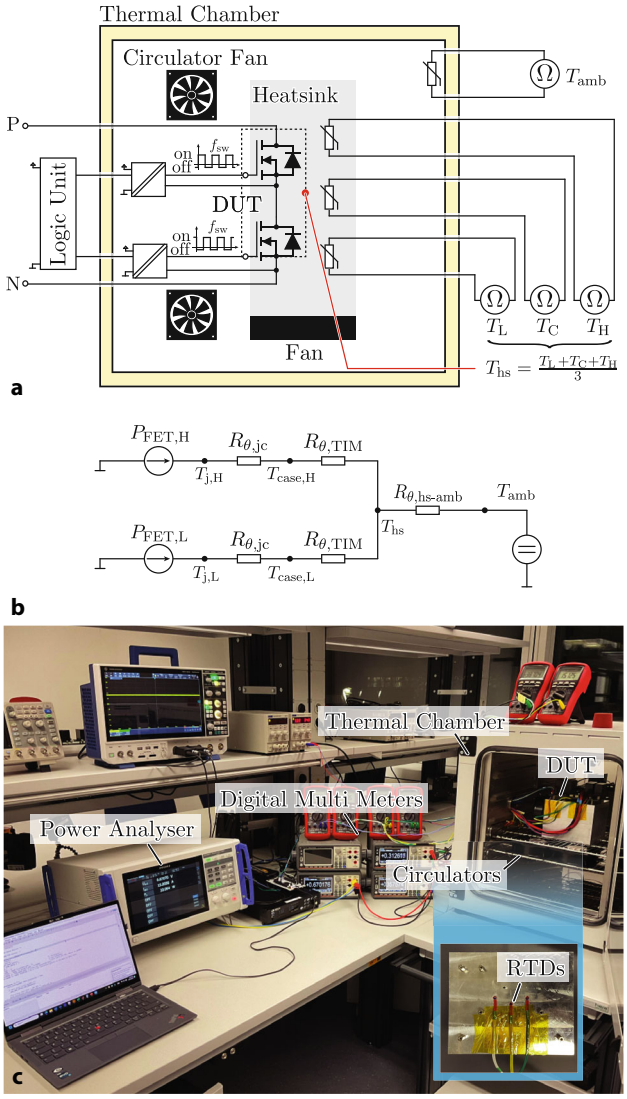

Fig. 4 **a** Measurement setup for the bridge-leg characterization, including three device-proximal temperature sensors T_L, T_C, and T_H, one ambient sensor T_{amb}, and two circulator fans, ensuring a homogeneous temperature within the chamber. The device under test (DUT) is mounted on a heat sink with a high-temperature fan capable of adequate heat dissipation. **b** Equivalent thermal network circuit model. **c** Setup appearance with measurement instruments. Complete list of the instruments and accuracy is in Appendix

2.2 Measurement setup

To facilitate measurements under elevated ambient temperatures, the hardware demonstrator is placed within a thermal chamber capable of regulating the ambient temperature; see Fig. 4 and [43] for the details on the chamber. The constructed half-bridge PCB is mounted onto a heat sink, connected to PE for safety considerations, and equipped with a fan. In addition to the heatsink's fan, there are two circulator fans employed within the chamber to guarantee uniform temperature distribution. The inside of the thermal chamber is thermally isolated from outside, and the temperature is controlled by the function of the thermal chamber. It is essential to mention that the complete setup, including the fans, is designed to operate at high temperatures of up to 150 °C.

The selected cooling system has a low thermal resistance of $R_{\theta,\mathrm{hs-amb}} = 0.15\,\mathrm{K/W}$, thereby guaranteeing a minimal thermal gradient between the ambient temperature within the chamber and the heatsink, i.e. $T_{\mathrm{amb}} \approx T_{\mathrm{hs}}$. To derive the actual heat sink temperature, we take the average of the three employed sensors as shown in Fig. 4a, i.e. $T_{\mathrm{hs}} = (T_{\mathrm{L}} + T_{\mathrm{C}} + T_{\mathrm{H}})/3$, which are affixed near the transistors using thermal epoxy [44]. Sil-Pad 2000 is employed as TIM [45], achieving a thermal resistance of around $R_{\theta,\mathrm{TIM}} = 0.92\,\mathrm{K/W}$ between the heat sink and the case of the power transistor. The device's junction-to-case thermal resistance is approximately equal to $R_{\theta,\mathrm{jc}} = 0.35\,\mathrm{K/W}$ for the considered 20 mΩdevices. By employing a heatsink with a thermal resistance of 0.13 K/W [46], the majority of the heat flow occurs through the heatsink, and the thermal circuit network is depicted in Fig. 4b. Thus, the junction temperatures of the devices can be estimated based on the device losses $P_{\mathrm{FET,H}}$ and $P_{\mathrm{FET,L}}$ with

$$\begin{aligned} T_{\mathrm{j,H}} &= P_{\mathrm{FET,H}}\,(R_{\theta,\mathrm{jc}} + R_{\theta,\mathrm{TIM}}) + T_{\mathrm{hs}}, \\ T_{\mathrm{j,L}} &= P_{\mathrm{FET,L}}\,(R_{\theta,\mathrm{jc}} + R_{\theta,\mathrm{TIM}}) + T_{\mathrm{hs}}. \end{aligned} \tag{2}$$

Assuming the device losses in the high-side and low-side FETs are equal, i.e., $P_{\mathrm{FET}} = P_{\mathrm{FET,H}} = P_{\mathrm{FET,L}}$, the junction temperatures of the high-side and low-side FETs are also equal, resulting in $T_{\mathrm{j}} = T_{\mathrm{j,H}} = T_{\mathrm{j,L}}$. It should be noted that $R_{\theta,\mathrm{TIM}}$ constitutes the majority of the thermal resistance due to its relatively larger value; therefore, minor differences between $R_{\theta,\mathrm{TIM}}$ due to different devices do not significantly impact the result. The desired junction temperature T_{j} required within the characterization can be achieved by changing the ambient temperature $T_{\mathrm{amb}} \approx T_{\mathrm{hs}}$, as

$$T_{\mathrm{j}} = P_{\mathrm{FET}}\,(R_{\theta,\mathrm{jc}} + R_{\theta,\mathrm{TIM}}) + T_{\mathrm{hs}}, \tag{3}$$

assuming given device losses P_{FET}.

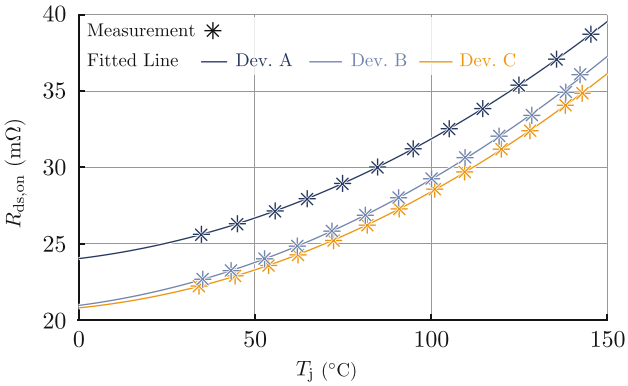

Fig. 5 Measured on-state resistance $R_{\mathrm{ds,on}}$ of single device across junction temperature T_{j} for Dev. A, Dev. B, and Dev. C. The results of the approximation (4) are shown with a continuous line, and the fitting coefficients are given in Table 2

3 Bridge-leg characterization

Within this section, we present the measurement results across varying junction temperatures T_{j} and DC-link voltage V_{DC} for on-state resistance $R_{\mathrm{ds,on}}$, output charge Q_{oss} and gate charge Q_{g}. From the gate charge we obtain Miller charge $Q_{\mathrm{M}} = Q_{\mathrm{g}} - Q_{\mathrm{g0}}$ where $Q_{\mathrm{g0}} = Q_{\mathrm{g}}(V_{\mathrm{DC}} = 0)$. We provide the measurements for the three considered MOSFETs.

3.1 On-state resistance characterization

To characterize the relationship between on-state resistance $R_{\mathrm{ds,on}}$ and junction temperature T_{j}, we employed a thermal chamber to control the ambient temperature T_{amb}. Once the desired thermal equilibrium was established, ensuring minimal disparity between the junction temperature T_{j} and the heatsink temperature T_{hs}, we take the measurement of the $R_{\mathrm{ds,on}}$. Keeping both transistors turned on and allowing a current of $I_{\mathrm{dc}} = 0.9\,\mathrm{A}$ through them, we achieved a balance that minimized self-heating, thereby maintaining a negligible temperature difference between the heatsink and junction and ensured sufficient voltage drop for accurate V_{DC} measurement. The on-state resistance results with $R_{\mathrm{ds,on}} = \frac{1}{2} V_{\mathrm{DC}} / I_{\mathrm{DC}}$.

Measurements were carried out across a temperature range from 30 °C to 150 °C for all three devices (Dev. A, Dev. B, and Dev. C), with the results shown in Fig. 5. It was observed that Dev. B and Dev. C exhibited nearly identical $R_{\mathrm{ds,on}}$ values at room temperature, whereas Dev. A demonstrated a roughly 15% higher $R_{\mathrm{ds,on}}$. A notable increase in $R_{\mathrm{ds,on}}$ was observed with rising junction temperatures T_{j}, surging by over 50% at 150 °C. To accurately model the temperature dependency, a quadratic fit is employed as

$$R_{\mathrm{ds,on}}(T_{\mathrm{j}}) = \gamma_0 + \gamma_1\, T_{\mathrm{j}} + \gamma_2\, T_{\mathrm{j}}^2, \tag{4}$$

with the coefficients γ_0, γ_1, and γ_2 detailed in Table 2.

Tab. 2 Fitting coefficients for Dev. A, Dev B, and Dev. C

Device	Coefficients for approximation							
	γ_0 (mΩ)	γ_1 (mΩ/K)	γ_2 (mΩ/K^2)	α_{oss}	β_{oss}	Q_{g0} (nC)	α_g	β_g
Dev. A	24.02	0.028	5.05×10^{-4}	7.93	0.48	96.34	0.11	0.74
Dev. B	20.94	0.030	5.25×10^{-4}	8.82	0.49	156.49	0.34	0.54
Dev. C	20.78	0.024	5.27×10^{-4}	17.06	0.37	162.25	0.20	0.51

3.2 Output charge characterization

The characterization of the MOSFETs output charge Q_{oss} is based on ZCS experiments [12, 47]. The switch node remains open, and the half-bridge operates at a predefined switching frequency f_{sw} with a duty cycle of 25%, as shown in Fig. 10 for Dev. A. Upon switching on the transistor, the stored energy is dissipated as the C_{oss} discharges from V_{DC} to 0, while the C_{oss} of the complementary device charges from 0 to V_{DC}. Consequently, the DC supply needs to provide the associated bridge-leg losses given by

$$P_{DC} = V_{DC} I_{DC} = V_{DC}\left[f_{sw}\left(2Q_{oss} + C_{par} V_{DC}\right) + \frac{V_{DC}}{R_{disch}}\right], \quad (5)$$

where a device-independent loss contribution is added by the discharge resistor R_{disch} and parasitic capacitance C_{par}, see **Sec.** 2.1. Finally, the output charge can be derived from the DC-link measurements with

$$Q_{oss} = \frac{1}{2f_{sw}}\left(I_{DC} - \frac{V_{DC}}{R_{disch}}\right) - \frac{C_{par}}{2} V_{DC}. \quad (6)$$

To achieve the desired junction temperature T_j for the experiments, the switching frequency f_{sw} is adjusted to ensure each device dissipates 10 W, equating to $V_{DC} I_{DC} - V_{DC}^2 / R_{disch} = 2P_{FET} = 20\,\text{W}$, which introduces a temperature difference of $\Delta T = T_j - T_{hs} = 13\,°\text{C}$ based on (3). This necessitates altering the f_{sw} for each voltage level tested to maintain 10 W of dissipation, thereby setting the thermal chamber's temperature to $T_{amb} = T_j - \Delta T$. For targeted junction temperatures of 45 °C, 85 °C, and 125 °C, this results in ambient temperatures of 32 °C, 72 °C, and 112 °C, respectively. The DC-link voltage was varied between 200 V and 950 V, leading to a switching frequency range between 30 kHz to 430 kHz.

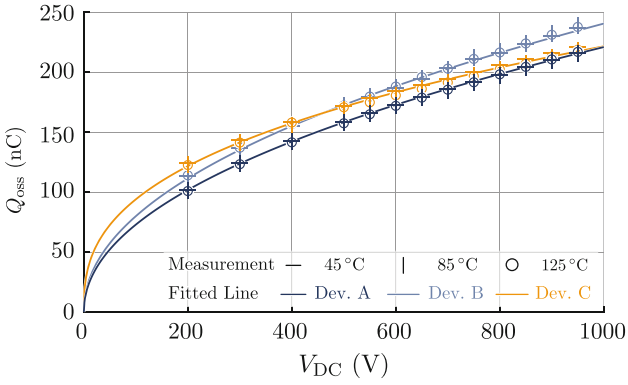

Fig. 6 Measured output charge Q_{oss} of single device for Dev. A, Dev B, and Dev. C across DC-link voltage V_{DC} under three junction temperature conditions T_j = 45 °C, 85 °C, 125 °C to show temperature invariant characteristics. The results of the approximation (7) are shown with a continuous line, and the fitting coefficients are given in Table 2

The findings in Fig. 6 reveal the following conclusion: Q_{oss} increases with voltage based on a non-linear relationship, as also shown in [48–50], but remains unaffected by junction temperature. Dev. A exhibited the lowest Q_{oss}, consistent with its higher $R_{ds,on}$, suggesting a smaller chip area compared to the other devices analyzed. At lower voltages, Dev. B and C showed marginally higher Q_{oss} charges; Dev. B maintained this disparity across the voltage spectrum, whereas Dev. C's Q_{oss} converged with Dev. A's at higher voltages. To quantitatively represent our data, we applied a curve fit to the output charge as

$$Q_{oss}(V_{DC}) = \alpha_{oss} V_{DC}^{\beta_{oss}}, \quad (7)$$

grounded in semiconductor physics [48–50], with coefficients α_{oss} and β_{oss} detailed in Table 2.

3.3 Gate charge characterization

We utilized the same hardware configuration and operating points as in Sect. 3.2 to characterize the gate charge Q_g. The power demand of the gate driver comprising gate charge and gate driver losses and it can be obtained by $P_{GD} = V_p I_p + V_n I_n$, where the positive and negative gate supply voltages and currents V_p, I_p, V_n, and I_n are measured in situ, see Fig. 2. It is important to note that P_{GD} depends on the switching frequency f_{sw}; the faster the switching frequency, the higher the gate losses. However, even when the MOSFET is not operated, i.e., when $f_{sw} = 0$, the gate driver IC consumes a certain baseline power P_{GD0} to supply its internal circuitry, which varies between 23 mW and 28 mW and must be measured for each ambient/junction temperature. To estimate the gate charge Q_g, the baseline power P_{GD0} is subtracted from the P_{GD}, which is measured for a given V_{DC} and a set f_{sw}. Therefore, the gate charge is calculated as

$$Q_g = \frac{(P_{GD} - P_{GD0})/f_{sw}}{V_g}, \quad (8)$$

where $V_g = V_p - V_n = 18.8\,\text{V}$ is consistently maintained throughout the experiments thanks to the voltage stabilizer integrated into the gate drive circuit.

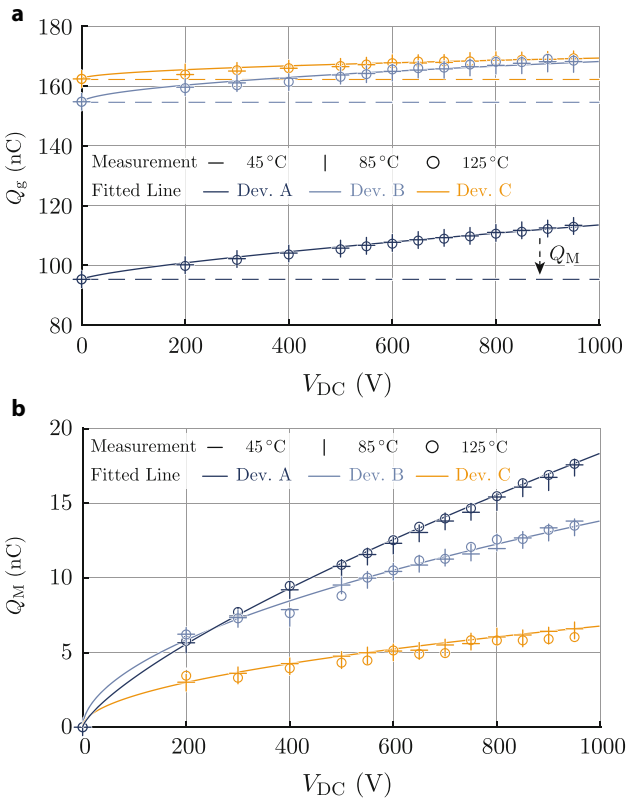

Fig. 7 Measurement results for **a** gate charge Q_g and **b** increase of the Miller charge Q_M due to DC-link voltage of Dev. A, Dev B, and Dev. C across DC-link voltage V_{DC} under three different junction temperatures 45 °C, 85 °C, 125 °C, showing temperature invariant characteristics. The results of the approximation (9) are plotted with a continuous line, and the fitting coefficients are given in Table 2

To quantify our measurement results, we fit the measurement data to

$$Q_g(V_{DC}) = Q_{g0} + \alpha_g V_{DC}^{\beta_g}, \tag{9}$$

with coefficients provided in Table 2. The charge $Q_{g0} = Q_g(0)$ represents the gate charge at zero DC-link voltage $V_{DC} = 0$, allowing for the estimation of the Miller charge as $Q_M = Q_g - Q_{g0} = \alpha_g V_{DC}^{\beta_g}$, depicted in Fig. 7b. These measurement results offer valuable insights into the performance of the studied transistors, showing that Dev. A possesses the lowest Q_{g0}, which is advantageous for soft switching applications, suggesting its manufacturer has optimized the gate structure for SiC MOSFETs. Conversely, Q_M of Dev. A exhibits the strongest dependency on V_{DC} among all devices, whereas Dev. C shows the lowest V_{DC} dependency. Dev. B and C display similar Q_{g0} values, indicating subtle differences in their gate charge characteristics.

4 Measurement-based figures of merit

Utilizing the measured data for on-state resistance $R_{ds,on}$ versus junction temperature T_j, the gate charge Q_{g0}, and the output charge Q_{oss} and Miller charge Q_M against DC-link voltage—affirmed to be independent of temperature—we obtained the FOMs listed in Table 1. Because $R_{ds,on}$ and charges Q_{g0}, Q_{oss}, Q_M exhibit positive correlation with semiconductor device losses, i.e., conduction and switching losses, the characterized parameters shown in Table 2 are therefore positive correlation with the losses. Consequently, larger coefficients indicate higher losses and thus lower performance. These characterized parameters are substituted into the denominator of the respective FOMs, ensuring that larger FOM values correspond to lower losses and therefore higher performance.

These FOMs are plotted against the DC-link voltage V_{DC} and junction temperature T_j to illustrate variations across different manufacturers, namely for Dev. A, B, and C, see Fig. 8. The analysis revealed that FOM_I exhibits remarkable consistency across the measured devices. As FOM_I is defined using on Q_{oss}, consequently it indicates hard-switching losses [47]. Therefore, the results for FOM_I suggest that SiC devices from various manufacturers can be replaced in hard-switched converters (with negligible overlap losses) without sacrificing performance. However, differences emerged for FOM_{II} and FOM_{III}. For example, FOM_{II} for Dev. A is approximately 33% higher than that for Dev. B and C. This discrepancy aligns with Dev. A's previously noted lower gate charge Q_{g0} (refer to Fig. 7a). Since FOM_{II} is obtained using Q_{g0}, it consequently indicates the performance of devices operating under synchronous rectification, which underscores the need for thorough evaluation when considering second sourcing of associated power devices. Specifically, substituting Dev. A for Dev. B or C could increase losses and gate driver power. It should be noted that FOM_{II} is independent of V_{DC} as it is defined based on Q_{g0} that is measured for $V_{DC} = 0$. Finally, as FOM_{III} is defined using Miller charge Q_M, it therefore indicates the performance of hard-switched converters where dv/dt associated loss components (overlap losses) are significant. A superior performance potential for Dev. C over Dev. A and B can be deduced from measurement-based FOMs. This finding suggests careful consideration when exploring second sourcing options for devices in converter systems with significant dv/dt switching loss component.

Fig. 9 reports results for a single operating point of $V_{DC} = 800\,V$ and two different junction temperatures of $T_j = 65\,°C$ and $T_j = 125\,°C$. As discussed for Fig. 8, there is a consistency over devices for FOM_I, whereas for FOM_{II} or FOM_{III}, either Dev. A or Dev. C perform the best. In addition, we provide dv/dt measurements in Fig. 9d for the same operating points, which are obtained as indicated in Fig. 10 using *Rohde & Schwarz MXO 5* oscilloscope and passive probe *RT-ZL04*. The dv/dt values match the trend of FOM_{III}, justifying its relation to overlap losses.

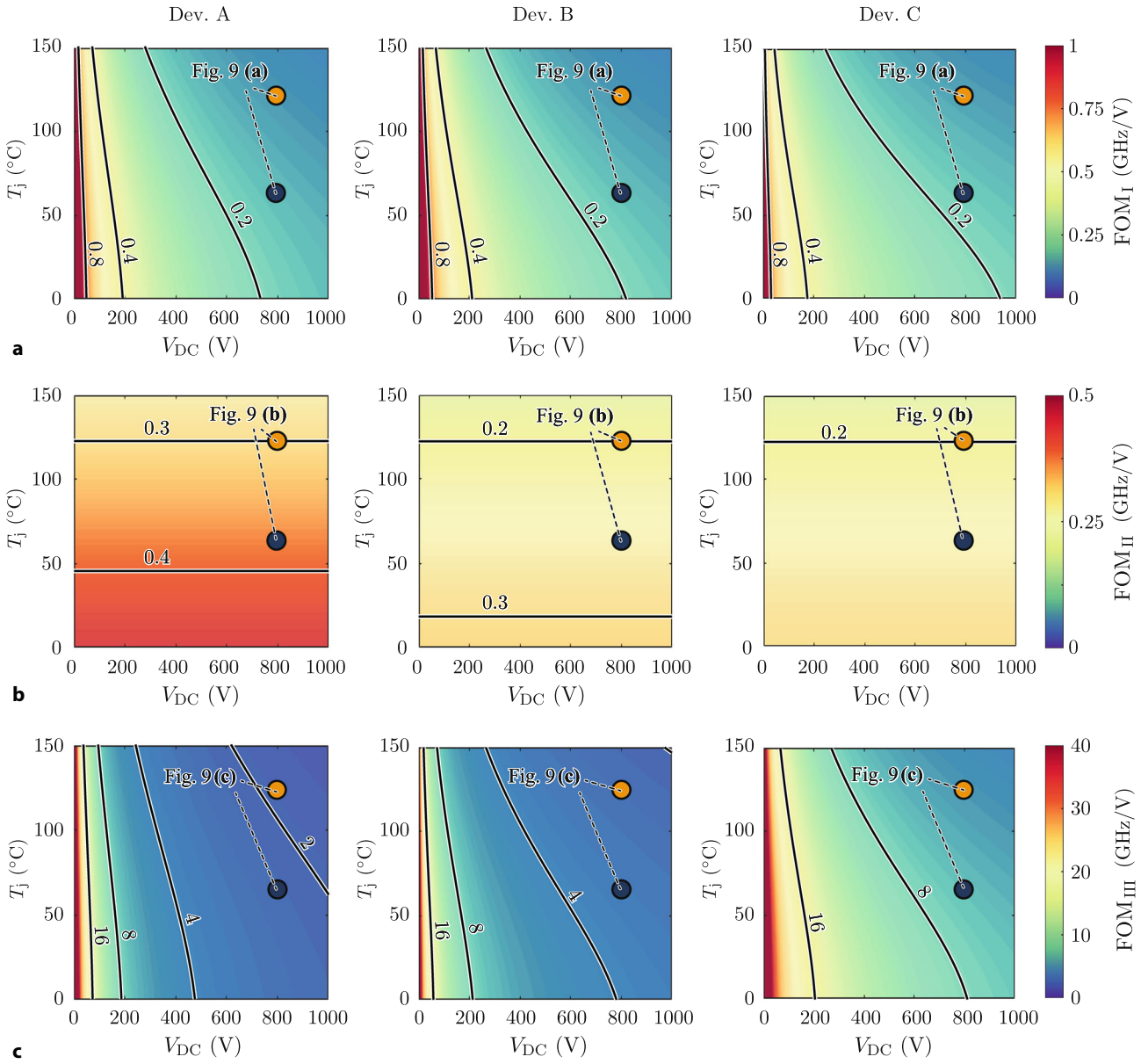

Fig. 8 Figures of Merit (FOMs) obtained from measurement results of $R_{ds,on}$, Q_{oss}, Q_{g0} and Q_M for Dev. A, B, and C across junction temperature T_j and DC-link voltage V_{DC}: **a** FOM_I, **b** FOM_{II} and **c** FOM_{III}. See Table 1 for the definition of the FOMs

5 Conclusions

This paper offers a detailed, measurement-driven analysis of Silicon Carbide (SiC) devices from three distinct manufacturers designated as Dev. A, B, and C. The primary aim of this study is to provide design engineers with comparative insights into the performance of SiC devices across various manufacturers, assessing the implications of second sourcing on design complexity. To facilitate this evaluation, we have developed a high-temperature experimental setup capable of characterizing TO-247-4 packaged DUTs, enabling us to compare the measured on-state resistance $R_{ds,on}$, output charge Q_{oss}, and gate charge Q_g, under constant (load-independent) gate drive voltages. The devices were characterized at temperatures up to 150 °C for $R_{ds,on}$ and up to 125 °C for Q_{oss} and Q_g. With these measurements, we empirically show the temperature independence of the charges Q_{oss} and Q_g. Further, utilizing the measured data for $R_{ds,on}$, Q_{oss}, and Q_g, we construct Figures of Merit (FOMs) as a function of DC-link voltage V_{DC} and junction temperature T_j. Our findings reveal that an FOM indicating the performance of a hard-switched converter system (with negligible overlap losses) has minimal disparities between devices. However, gate charge-based FOMs vary substantially, underscoring the critical importance when selecting SiC devices for synchronous rectification or in high-current operation, causing substantial overlap losses, as also verified by dv/dt measurements.

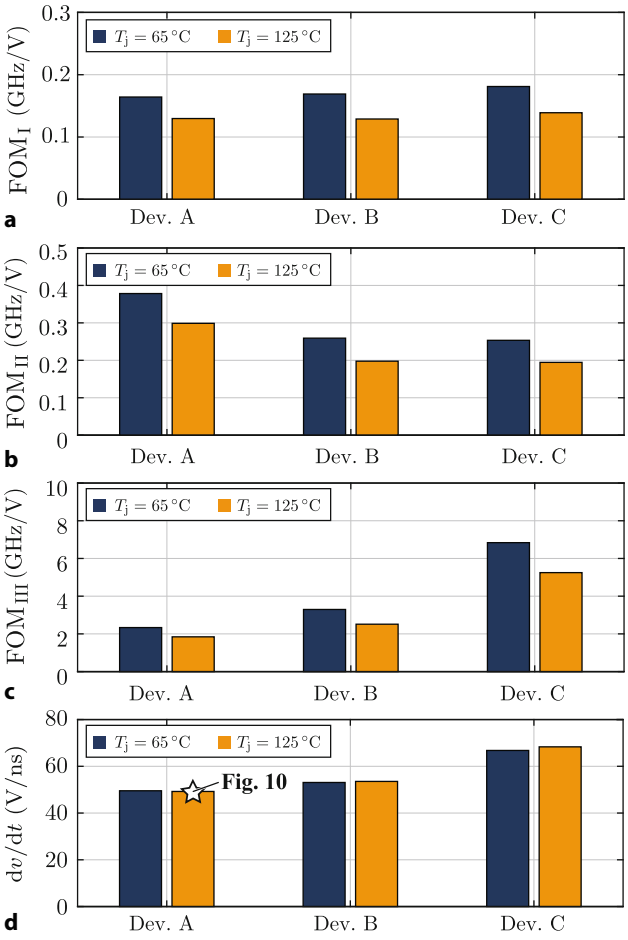

Fig. 9 Comparison of **a** $\mathrm{FOM_I}$, **b** $\mathrm{FOM_{II}}$, **c** $\mathrm{FOM_{III}}$ and **d** $\mathrm{d}v/\mathrm{d}t$, for the operating point where $V_{DC} = 800\,V$ at two different junction temperatures $T_j = 65\,°C$ and $T_j = 125\,°C$

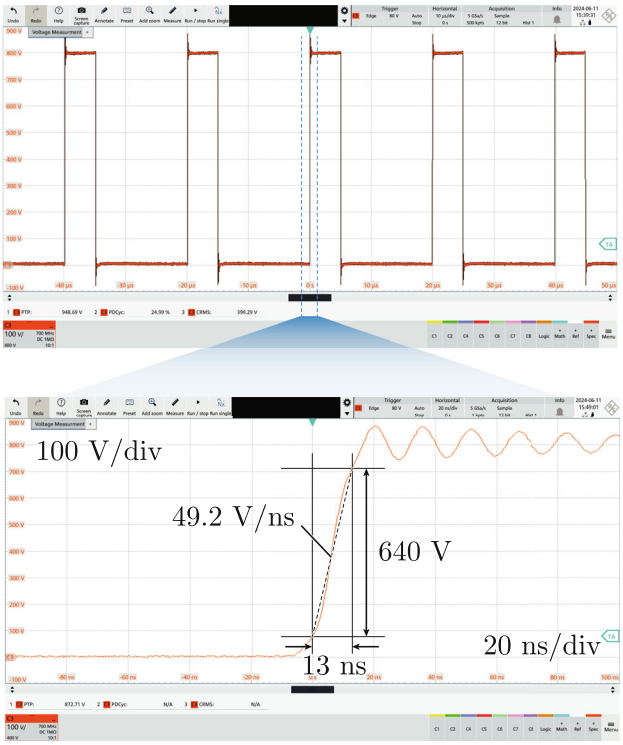

Fig. 10 Switch node voltage measurement in ZCS operation. The $\mathrm{d}v/\mathrm{d}t$ is approximated assuming a linear voltage rise from 10% to 90% of the DC link voltage. The shown measurement corresponds to Dev. A operating at $V_{DC} = 800\,V$, $f_{sw} = 50\,kHz$ and a duty cycle of 0.25

Our future research will focus on thermal characterization of bridge-legs including overlap losses and development of rapid power semiconductor loss evaluation methods based on switching transients, $\mathrm{d}v/\mathrm{d}t$ behavior, and transient waveform analysis.

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6 Appendix: Measurement instruments and error control

This appendix describes the measurement equipment and error control used for the characterizations.

6.1 Temperature measurement

Throughout the whole characterization process, *TE Connectivity CLASS AA RTD PT1000* was utilized as a temperature sensor. The resistance R_m of the sensor was measured using digital multi meter (DMM) *Brymen 869s*, and the measured temperature T_m was obtained using the RTD conversion formula in the case $T_m > 0$ [51]:

$$T_m = \frac{-R_0 a + \sqrt{(R_0 a)^2 - 4R_0 b(R_0 - R_m)}}{2R_0 a}, \tag{10}$$

where $a = 3.9083 \times 10^{-3}$, $b = -5.775 \times 10^{-7}$ and $R_0 = 1000\,\Omega$. According to the datasheet [51], the measurement error of the RTD itself is expressed as

$$\Delta T_{m,RTD} = \pm(0.1 + 0.0017 \times T_m). \tag{11}$$

The error of the DMM is represented by the error propagation using (10) as

$$\Delta T_{\mathrm{m,DMM}} = \pm \left| \frac{\partial T_{\mathrm{m}}}{\partial R_{\mathrm{m}}}(R_{\mathrm{m}}) \right| \Delta R_{\mathrm{m}}, \tag{12}$$

where ΔR_{m} consists of a reading error of 0.07% Rdg. and a full scale error of 0.2 Ω, and can be derived from the general form of the measurement error:

$$\Delta X_{\mathrm{m}} = \mathrm{F.S.} + \mathrm{Rdg.} \times X_{\mathrm{m}}, \tag{13}$$

where X_{m} is generalized measured parameter. The errors of $\Delta T_{\mathrm{m,RTD}}$ and $\Delta T_{\mathrm{m,DMM}}$ are calculated as follows. First, measured R_{m} is substituted into (10), from which we obtain T_{m}. Then, T_{m} is substituted into (11) to derive $\Delta T_{\mathrm{m,RTD}}$. $\Delta T_{\mathrm{m,DMM}}$ are calculated by substituting R_{m} and ΔR_{m} into (12), which finally leads to total error as

$$\Delta T_{\mathrm{m}} = \Delta T_{\mathrm{m,RTD}} + \Delta T_{\mathrm{m,DMM}}, \tag{14}$$

with the highest measurement temperature of 150 °C corresponding to $\Delta T_{\mathrm{m}} = \pm 0.69\,^{\circ}\mathrm{C}$, and the lowest measurement temperature of 30 °C corresponding to $\Delta T_{\mathrm{m}} = \pm 0.20\,^{\circ}\mathrm{C}$.

6.2 $R_{ds,on}$ measurement

For the measurement of $R_{\mathrm{ds,on}}$, the voltage and the current over the DUT were measured using a high precision digital multi meter *GW Instek GDM 9060*. During characterization, the voltage range can be fixed at 100 mV and the current range at 1 A according to the characterization procedures. The voltage measurement error ΔV_{m} is 0.009% Rdg. + 0.0065% F.S. and the current measurement error ΔI_{m} is 0.1% Rdg. + 0.01% F.S. under the measurement condition[52]. Since measured value $R_{\mathrm{ds,on,m}}$ was calculated as

$$R_{\mathrm{ds,on,m}} = \frac{V_{\mathrm{m}}}{I_{\mathrm{m}}}, \tag{15}$$

the total error of $R_{\mathrm{ds,on}}$ is estimated as

$$\begin{aligned} \Delta R_{\mathrm{ds,on,m}} = &\pm \left| \frac{\partial R_{\mathrm{ds,on,m}}}{\partial V_{\mathrm{m}}}(V_{\mathrm{m}}, I_{\mathrm{m}}) \right| \Delta V_{\mathrm{m}} \\ &\pm \left| \frac{\partial R_{\mathrm{ds,on,m}}}{\partial I_{\mathrm{m}}}(V_{\mathrm{m}}, I_{\mathrm{m}}) \right| \Delta I_{\mathrm{m}}, \end{aligned} \tag{16}$$

where ΔV_{m} and ΔI_{m} are calculated by (13). The calculated maximum measurement error of ±0.05 mΩat the temperature of 150 °C resulting in that the deviation from the fitting curve is hardly observable in Fig. 5 due to this level of precision.

6.3 $Q_{\mathrm{oss}}, Q_{\mathrm{g}}$ and Q_M measurement

For the characterization of each charge $Q_{\mathrm{oss}}, Q_{\mathrm{g}}$ and Q_{M}, the voltage and current of the half-bridge were measured using the voltage module *U7005* with 0.02 % Rdg. + 0.03 % F.S. and current sensor *CT6872* with 0.05 % Rdg. + 0.0202 % F.S. of the power analyzer *HIOKI PW8001*[53]. To ensure measurement accuracy, the current sensor was wound with a measurement wire eight times. Additionally, the switching frequency was measured using spectrum analyzer function of oscilloscope *Rohde & Schwarz MXO 5*.

As described in Sect. 3.2 and Sect. 3.3, the characterization of each charge is performed by dividing the power consumption, obtained from the half-bridge DC bus voltage and current measurements, by the switching frequency. For the same power consumption, an increase in switching frequency reduces the energy consumed per switching cycle, However, the error rate should remain constant. Thus, we assume that the measured switching frequency is the true value without error and calculate the relative error excluding the frequency. The frequency measurement accuracy of the oscilloscope $\Delta f_{\mathrm{sw,m}}$ is $0.02\,\mathrm{ppm} \times \mathrm{f_{sw,m}} + 1.1\,\mu\mathrm{Hz}$, resulting in a charge error $\Delta Q = \left| \frac{\partial Q}{\partial f_{\mathrm{sw,m}}} \right| \Delta f_{\mathrm{sw,m}} < 0.001\,\mathrm{nC}$, which is negligible and supports the aforementioned assumption.

In the characterization of Q_{oss}, the indirect measurement parameters are denoted as

$$x_{\mathrm{m}} = [V_{\mathrm{DC,m}}, I_{\mathrm{DC,m}}, V_{\mathrm{disch,m}}, I_{\mathrm{disch,m}}, C_{\mathrm{par,m}}]. \tag{17}$$

The relative measurement error of $\Delta Q_{\mathrm{oss}}/Q_{\mathrm{oss}}$ is expressed as

$$\frac{\Delta Q_{\mathrm{oss}}}{Q_{\mathrm{oss}}} = \frac{\frac{1}{2f_{\mathrm{sw,m}}} |\Delta f(x_{\mathrm{m}})| + |\Delta g(x_{\mathrm{m}})|}{\frac{1}{2f_{\mathrm{sw,m}}} f(x_{\mathrm{m}}) + g(x_{\mathrm{m}})}, \tag{18}$$

where f and g correspond to the functions derived from (6) as

$$f(x_{\mathrm{m}}) = I_{\mathrm{DC,m}} - \frac{V_{\mathrm{DC,m}}}{V_{\mathrm{disch,m}}/I_{\mathrm{disch,m}}}, \tag{19}$$

$$g(x_{\mathrm{m}}) = -V_{\mathrm{DC,m}} C_{\mathrm{par,m}}/2. \tag{20}$$

The errors associated with these functions Δf and Δg, are given by

$$\Delta f(x_{\mathrm{m}}) = \sum_{i=1}^{5} \left| \frac{\partial f}{\partial x_{\mathrm{m},i}}(x_{\mathrm{m}}) \right| \Delta x_{\mathrm{m},i}, \tag{21}$$

$$\Delta g(x_{\mathrm{m}}) = \sum_{i=1}^{5} \left| \frac{\partial g}{\partial x_{\mathrm{m},i}}(x_{\mathrm{m}}) \right| \Delta x_{\mathrm{m},i}, \tag{22}$$

where

$$\Delta x_{\mathrm{m}} = [\Delta V_{\mathrm{DC,m}}, \Delta I_{\mathrm{DC,m}}, \Delta V_{\mathrm{disch,m}}, \Delta I_{\mathrm{disch,m}}, \Delta C_{\mathrm{par,m}}]. \tag{23}$$

$\Delta C_{\mathrm{par}} = \pm 0.1\,\mathrm{pF}$ is substituted as the least significant digit of the C_{par} measurement, and other parameters of Δx_{m} are derived by (13) according to the range settings of the power analyzer.

As a result of the above calculations, the maximum relative error of Q_{oss} is 2.3 % at a voltage of 950 V corresponding to ±5.4 nC. The relative error of Q_g and Q_M can be derived in same manner, resulting in the maximum relative error is 0.66 % at voltage of 950 V corresponding to ±1.1 nC. Due to these errors, measurement variance can be observed in Fig. 7b for Q_M which has a smallest range of 20 nC, while for Q_{oss} and Q_g, the variance from the fitted curve is hardly noticeable in Fig. 6 and 7a since their errors are small relative to their ranges.

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Dr. Mirić has authored over 40 scientific papers in international journals and conference proceedings and holds seven patents. He has presented three educational seminars at leading international conferences and has received five IEEE Transactions and Conference Prize Paper Awards.