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Modulation in Voltage Source Inverters: an Algebraic Approach

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ABSTRACT Pulse width modulation in voltage source inverters with an arbitrary number of phases is analyzed in this paper. The problem is treated as purely algebraic, without any use of space vectors. Regardless of avoiding space vectors, the same results are achieved. It is shown that the problem of determining duty ratio values does not have a unique solution, and that there is one degree of freedom to choose one duty ratio, but within a limited range. Limits of the range are derived. Feasibility constraints for the required set of line voltages are derived, reducing to the requirement that the highest of the line voltages should be lower than the DC bus voltage. The analysis is illustrated in cases varying from two to five phases, and experimentally verified in the case of three phases. The method is simple and could be applied to any number of phases, even for the voltages that are not sinusoidal.

INDEX TERMS Applied Algebra, Multiphase, Power Electronics, Pulse Width Modulation, Pulse Width Modulation Inverters, Space Vector Pulse Width Modulation, Voltage Source Inverters.

I. INTRODUCTION

This paper addresses modulation in general n -phase voltage source inverter depicted in Fig. 1. In the inverter, upper switches S_k are operated such that they are on during $d_k T_S$, where d_k is the duty ratio, while T_S is the switching period. Lower switches, labeled \bar{S}_k are operated complementarily, being off while S_k is on, and vice versa, thus their duty ratio is $1 - d_k$. Index k , $k \in \{1, \dots, n\}$ indicates the inverter phase leg the variables apply to.

Duty ratio values characterize the modulation process in its low-frequency part, since they are defined over a switching period. In that sense, the modulation process could be divided in the frequency scale to a low-frequency part, below and at the switching frequency, and the high-frequency part, above the switching frequency. Low-frequency part is essential in the energy transfer, as it should provide the load with average values of the line voltages with adequate amplitude, frequency, and possibly shape. Also, low-frequency part of the modulation process can strongly affect the high-frequency part, since it can disable switching in an inverter leg during a part of the line period, completely annulling the high-frequency spectrum that the inverter leg generates. On the other hand, the high-frequency part of the modulation process affects the energy transfer only through the parasitic effect of losses, and in a minor part by electromagnetic interference.

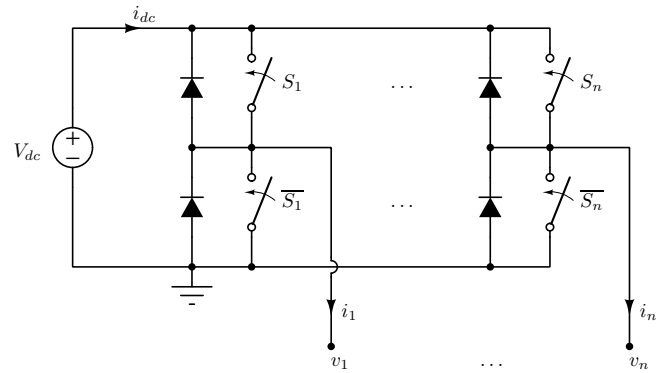


FIGURE 1. Voltage source inverter, n -phase.

In the analysis of the modulation process, we focus to its low-frequency part, determining unknown duty ratio values d_k for n phases. Historically, this problem has been approached by applying pulse width modulation first, but the resulting method was not able to extract the full potential to generate line voltages with the maximal amplitude. In [1], space vector modulation approach is proposed as a remedy, providing line voltage amplitudes equal to the DC bus voltage. This is achieved using space vector representation of

instantaneous values of voltages the inverter could generate. The analysis has also shown that the modulation strategy is not unique: there are two switch state combinations that provide the same zero vector, opening space for optimizations according to different criteria. Also, duty ratio values for the switches were the only result, without any suggestion where within a switching period the switch should be on or off. These degrees of freedom opened space for various modulation strategies, optimized according to different criteria.

After the space vector modulation has been introduced in [1], the fact that it is just a form of pulse width modulation was observed. Essentially, it is a method to create the pulse width modulation pattern, as shown in [2], where it was demonstrated that the same effect could be obtained only by adding appropriate zero-sequence AC components to the modulating signals. Several papers followed, [3]–[5], some using available freedom of choice to optimize the system performance, some discussing the modulation system realization details. Similar results are presented in [6], [7].

Available degrees of freedom opened space to a vast research work and resulting publications, summarized in early review papers like [8], [9], up to recent ones [10], and textbooks [11]. Available degrees of freedom were used to optimize the system parameters in many publications, like [12]–[15], besides the fact that almost all publications in modulation present some form of optimization. High frequency modulation effects are discussed in [16]–[19]. Overmodulation, which is a low-frequency phenomenon, is discussed in [20]–[22]. Dead-time is discussed in [23], [24], among other publications.

Regardless the available literature on the modulation topic, essential references for this paper are [1] and [2] and it would continue in that track, aiming for duty ratio values of the switches in the inverter legs and their relations to the average values of generated line voltages.

In this paper, modulation in voltage source inverters is approached in its low-frequency part as being an algebraic problem of determining n duty ratio values, from d_1 to d_n . It is shown that the same results as provided by [1], [2] could be achieved without any introduction of space vectors nor the zero-sequence AC components. The method is simple and straightforward, and provides a range in which d_1 should be chosen to fulfill the requirements of the average values of the line voltages. The choice of d_1 immediately implies other $n - 1$ duty ratio values. The freedom of choice for d_1 could be used to optimize the inverter performance according to desired criteria.

Proposed algorithm is simple, both in required mathematics and in its numerical implementation. The most complex operation in generating the modulation signals reduces to finding a minimum and/or a maximum of the phase voltages normalized to the inverter input voltage. Visualization of space vectors, sector identification, and subsequent harmonic analysis are completely avoided, reducing the method to elementary linear algebra in its straightforward implementation. Besides being simple, the algorithm is computation-

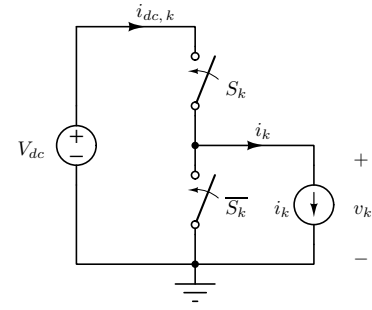


FIGURE 2. Inverter phase leg.

ally efficient, numerically stable, and easy to implement. Furthermore, the algorithm is easily generalized to arbitrary waveforms of generated voltages, just by providing adequate reference signals. Finally, the algorithm can be applied to inverters with any number of phases, making it a versatile solution for various multi-phase systems.

II. PROBLEM STATEMENT

In this section, the problem of determining d_k for $k \in \{1, \dots, n\}$ is stated as an algebraic problem.

A. THE INVERTER LEG

The inverter leg that corresponds to one phase of the inverter of Fig. 1 is presented in Fig. 2. It is assumed that the upper switch is turned on during $d_k T_S$ of the switching period T_S , while for the remaining of the switching period the lower switch is turned on. This results in the average of the leg output voltage of

$$\langle v_k \rangle = V_{dc} d_k \quad (1)$$

while the average of the input current is

$$\langle i_{dc,k} \rangle = i_k d_k. \quad (2)$$

The duty ratio limits are

$$0 \leq d_k \leq 1 \quad (3)$$

which will be used in the analysis that follows.

Introducing normalized averaged phase voltages as

$$m_k = \frac{\langle v_k \rangle}{V_{dc}} \quad (4)$$

we obtain that normalized averaged phase voltage referred to the negative bar of the input DC source determines the duty ratio it requires directly

$$d_k = m_k. \quad (5)$$

Considering the average of the phase voltage k , introduced as $\langle v_k \rangle$, to consist a DC component and a sinusoidal AC component at the fundamental frequency only, due to (3) the maximum of the AC component equals to one half of the DC link voltage, to $\frac{1}{2} V_{dc}$,

$$\langle v_k \rangle = \frac{1}{2} V_{dc} + \frac{1}{2} m V_{dc} \cos \left(\omega_0 t - (k-1) \frac{2\pi}{n} \right) \quad (6)$$

which is achieved for the modulation index $m = 1$. The modulation index, conventionally labeled as m , should not be confused with normalized phase voltages m_k , and

$$d_k = m_k = \frac{1}{2} + \frac{1}{2} m \cos \left(\omega_0 t - (k-1) \frac{2\pi}{n} \right) \quad (7)$$

represents (6) in its normalized form.

B. TWO/SINGLE-PHASE CASE

As a first case study, let us consider a single phase inverter, which in our nomenclature corresponds to two phase inverter, since there are two inverter legs, thus $n = 2$.

Consider duty ratio value for the first inverter leg

$$d_1 = \frac{1}{2} + \frac{1}{2} m \cos(\omega_0 t) \quad (8)$$

which provides the phase voltage DC component of $\frac{1}{2} V_{dc}$ and can provide the AC component up to the same amplitude.

On the other hand, for the remaining inverter leg consider the duty ratio with the same DC component, while the AC component has the same amplitude, but the opposite phase

$$d_2 = \frac{1}{2} + \frac{1}{2} m \cos(\omega_0 t - \pi) = \frac{1}{2} - \frac{1}{2} m \cos(\omega_0 t). \quad (9)$$

According to (5), corresponding normalized inverter output voltage is

$$m_{1,2} = d_1 - d_2 = m \cos(\omega_0 t) \quad (10)$$

which corresponds to the output voltage amplitude up to V_{dc} . So, everything seems to be as expected, the maximum of the generated voltage amplitude equals the DC link voltage. However, in the text that follows it will be shown that this is only one solution to this problem.

C. THREE-PHASE CASE

Applying the same methods, consider a three phase case, $n = 3$, which is of high practical interest. Assuming

$$d_1 = \frac{1}{2} + \frac{1}{2} m \cos(\omega_0 t) \quad (11)$$

$$d_2 = \frac{1}{2} + \frac{1}{2} m \cos \left(\omega_0 t - \frac{2\pi}{3} \right) \quad (12)$$

and

$$d_3 = \frac{1}{2} + \frac{1}{2} m \cos \left(\omega_0 t - \frac{4\pi}{3} \right) \quad (13)$$

resulting normalized value of the first line voltage is

$$m_{1,2} = \frac{1}{2} \left(\cos(\omega_0 t) - \cos \left(\omega_0 t - \frac{2\pi}{3} \right) \right) \quad (14)$$

which maps to the line voltage of

$$\langle v_{1,2} \rangle = \frac{\sqrt{3}}{2} V_{dc} \cos \left(\omega_0 t + \frac{\pi}{6} \right). \quad (15)$$

This corresponds to the line voltage amplitude of

$$V_m = \frac{\sqrt{3}}{2} V_{dc} \approx 0.866 V_{dc}. \quad (16)$$

The value is scaled down by $\frac{\sqrt{3}}{2} \approx 0.866$ in comparison to the expected maximal line voltage equal to V_{dc} , as achieved in the single phase case. This motivated space vector approach to increase the maximum of the generated line voltage amplitude for 15.5%. The same applies for the remaining two of the line voltages.

On the other hand, choosing

$$d_1 = \frac{1}{2} + \frac{1}{2} \cos \left(\omega_0 t + \frac{\pi}{6} \right) \quad (17)$$

and

$$\begin{aligned} d_2 &= \frac{1}{2} + \frac{1}{2} \cos \left(\omega_0 t + \frac{7\pi}{6} \right) \\ &= \frac{1}{2} - \frac{1}{2} \cos \left(\omega_0 t + \frac{\pi}{6} \right) \end{aligned} \quad (18)$$

provides the line voltage

$$\langle v_{1,2} \rangle = V_{dc} \cos \left(\omega_0 t + \frac{\pi}{6} \right) \quad (19)$$

in which the amplitude corresponds to the expected maximum of V_{dc} . Following the same logic, aiming the line voltage amplitude value of V_{dc} , the duty ratio for the third phase should be

$$d_3 = \frac{1}{2} + \frac{1}{2} \cos \left(\omega_0 t + \frac{\pi}{6} \right) \quad (20)$$

resulting in

$$\langle v_{2,3} \rangle = -V_{dc} \cos \left(\omega_0 t + \frac{\pi}{6} \right) \quad (21)$$

which has the same amplitude, equal to the expected maximum of V_{dc} , but the phase is not shifted for $\frac{2\pi}{3}$, instead it is π . Furthermore, this automatically provides

$$\langle v_{3,1} \rangle = 0 \quad (22)$$

which is a dependent variable, since all three of the line voltages should add up to zero.

This example indicates that the problem is in mutual linking of the phase voltages as they map to the line voltages. With six inverter legs it would be possible to achieve three voltages with the amplitude equal to V_{dc} and the appropriate phases, reducing the problem to three single-phase inverters. However, these voltages would not be three line voltages in our common notion, since they do not add one to another. Besides, such realization would be overly complex and expensive.

The insight provided by this example is that the problem in achieving three line voltages with the amplitude equal to the DC link voltage lays in mutual coupling of the phase voltages as they form line voltages, and that decoupling would remove the problem. The topic of coupled linear equations, since line voltages are just differences of phase voltages, is a typical problem of linear algebra.

D. PHASE VOLTAGES, LINE VOLTAGES, AND FUNDAMENTAL COMPONENTS OF PHASE VOLTAGES

Consider a system of n phases. Line voltages are defined as differences of the phase voltages

$$v_{j,k} = v_j - v_k \quad (23)$$

where $j \in \{1, \dots, n\}$ and $k \in \{1, \dots, n\}$ are flying indices. It should be noted here that adding the same value v_0 to all of the phase voltages would not change the line voltages since

$$v_{j,k} = (v_j + v_0) - (v_k + v_0). \quad (24)$$

Furthermore, a sequence of line voltages starting from $v_{1,2}$, $v_{2,3}$ and ending with $v_{n-1,n}$, $v_{n,1}$ according to the Kirchhoff's voltage law should add up to zero

$$\sum_{k=1}^{n-1} v_{k,k+1} + v_{n,1} = 0. \quad (25)$$

This means that for the phase voltages we have n independent voltages as input values of the analysis. On the other hand, in the sequence of line voltages only $n - 1$ are independent, since they should satisfy the constraint (25). In this manner, transformation from phase voltages to the line voltages is unique, n values of phase voltages provide n values of the sequential line voltages. On the other hand, line voltages cannot be transformed back to the phase voltages in a unique fashion, since only $n - 1$ of them are independent, and there is a degree of freedom materialized in v_0 of (24).

It is our convenience to have a set of phase voltages that corresponds to a given set of line voltages in a unique fashion. This could be achieved by adding a constraint that would eliminate any value of the zero-sequence component v_0 (24). Such additional requirement results in introduction of a set of fundamental phase voltages $v_{P,k}$ which satisfy the additional criterion that they add up to zero,

$$\sum_{k=1}^n v_{P,k} = 0. \quad (26)$$

Fundamental components of the phase voltages are free of the zero-sequence component v_0 , and they can be obtained from any set of phase voltages using

$$v_{P,k} = v_k - \frac{1}{n} \sum_{k=1}^n v_k. \quad (27)$$

E. AMPLITUDE LIMITS

In order to determine maximum of the phase voltage fundamental component amplitude that could be generated, our attention is restricted to sinusoidal output line voltages of the inverter. Let us consider an n -phase voltage system with fundamental components of the phase voltages given by

$$\langle v_{P,k} \rangle = V_{P,max} \cos \left(\omega_0 t - (k-1) \frac{2\pi}{n} \right) \quad (28)$$

for $k \in \{1, \dots, n\}$. Maximum of the generated voltage amplitude is limited by two phase voltages that are closest to be in

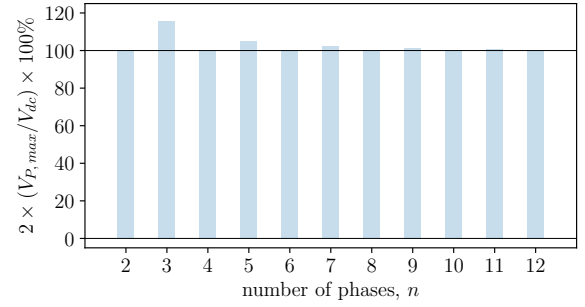


FIGURE 3. Maximum of the fundamental phase voltage amplitudes a function of the number of phases n .

the opposite phase, resulting in the highest line voltage, and its amplitude being equal to the DC bus voltage V_{dc} limits the amplitudes of the fundamental components of phase voltages. As the first of these phases we would always consider the first phase, for $k = 1$,

$$\langle v_{P,1} \rangle = V_{P,max} \cos(\omega_0 t). \quad (29)$$

At this point, the case for the number of phases n being even and the case for n being odd separate. For even n , there is always a phase voltage in the set having the opposite phase to the first one, which happens for $k - 1 = \frac{n}{2}$, where

$$\langle v_{P,k} \rangle = V_{P,max} \cos(\omega_0 t - \pi) = -V_{P,max} \cos(\omega_0 t) \quad (30)$$

which with (29) produces the line voltage amplitude equal to V_{dc}

$$\langle v_{1,k} \rangle = 2 V_{P,max} \cos(\omega_0 t) = V_{dc} \cos(\omega_0 t). \quad (31)$$

This results in maximal amplitudes of the phase voltage fundamental components of

$$V_{P,max} = \frac{1}{2} V_{dc} \quad (32)$$

in the case when n is even. In these cases, space vector modulation could not provide any gain in the amplitude, and direct pulse width modulation (7) discussed in II-B provides one solution for the duty ratio functions which results in the maximum of the amplitudes.

In the case of odd n , phase voltage amplitude is limited by two phase voltage fundamental components closest to the opposite. Let $n = 2l + 1$ be an odd number of phases, and consider phase voltages 1 and $l + 1$, as being closest to the opposite in phase, resulting in the line voltage

$$\langle v_{1,l+1} \rangle = V_{P,max} \left(\cos(\omega_0 t) - \cos \left(\omega_0 t - l \frac{2\pi}{n} \right) \right). \quad (33)$$

Using sum-to-product trigonometric identities we obtain

$$\langle v_{1,l+1} \rangle = -2 V_{P,max} \sin \left(l \frac{\pi}{n} \right) \sin \left(\omega_0 t - l \frac{\pi}{n} \right) \quad (34)$$

where the amplitude could be clearly identified as a factor not being dependent on $\omega_0 t$. Equating the amplitude with V_{dc} , the phase voltage amplitude is obtained as

$$V_{dc} = 2 V_{P,max} \sin \left(l \frac{\pi}{n} \right). \quad (35)$$

Having in mind that $l = \frac{n-1}{2}$, trigonometric transformations yield

$$V_{dc} = 2 V_{P, \max} \sin \left(\frac{\pi}{2} - \frac{\pi}{2n} \right) = 2 V_{P, \max} \cos \left(\frac{\pi}{2n} \right) \quad (36)$$

which finally produces

$$V_{P, \max} = \frac{V_{dc}}{2 \cos \frac{\pi}{2n}}. \quad (37)$$

In the case of an odd number of phases n , it is possible to achieve some gain in the output voltage amplitude using space vector modulation or injecting the zero-sequence AC component in modulating signals, which is the same in effect, but the method is different in derivation and computation.

Dependence of the phase voltage fundamental component amplitude maximum on the number of phases is shown in Fig. 3. As expected, there is no gain in comparison to the direct pulse width modulation (7) in cases when n is even, and there is some gain for odd values of n , the biggest for $n = 3$ where a gain of about 15.5% could be achieved. This gain drops rapidly for higher odd values of n . In the diagram of Fig. 3, phase voltage amplitudes are chosen to be depicted, since that for $n > 3$ the line voltages depend in amplitude on the choice of terminal phases, being the lowest for neighboring phases, and the largest for the phases being closest to the opposite.

From this point onward, normalized phase voltages would be assumed as their fundamental components

$$m_k = m \frac{V_{P, \max}}{V_{dc}} \cos \left(\omega_0 t - (k-1) \frac{2\pi}{n} \right) \quad (38)$$

and when the modulation index m is not explicitly stated it would be assumed that $m = 1$.

Up to this point, it has been assumed that the phase voltages are sinusoidal and that the input voltage V_{dc} is constant, which corresponds to the situation frequently analyzed in literature and encountered in practice. However, these assumptions are released in the analysis that follows, not being required at all: neither the phase voltages are required to be sinusoidal, neither the inverter input voltage needs to be constant. The analysis that follows provides the duty ratio values as they depend on m_k values. The m_k values are obtained as ratios of required values of the fundamental components of the phase voltages, void of the zero sequence component, and the inverter input voltage. These values can even be obtained using measured values of the inverter input voltage, actual at a given moment in time, whatever the reason for the input voltage variation is, including the load variations. Proposed algorithm would provide the duty ratio values that generate the required average values of the phase voltages out of the available inverter input voltage, anyhow. The input variables for this algorithm are the values of m_k . Now, the task is to determine the duty ratio values out of the required m_k values.

III. DUTY RATIO VALUES

Essential part of the problem posed in this paper is to determine duty ratio values that provide prescribed values of the

line voltages. This problem is addressed in this section using a purely algebraic approach.

A. DUTY RATIO REQUIREMENTS

Let us assume that we have n values of sequencing line voltages, by sequencing meaning that their indices follow one another closing the loop, that are required to obtain using a voltage source inverter. Also, let us assume that these values are normalized to V_{dc} . Out of these values, only $n-1$ are independent, since there is a constraint imposed by the Kirchhoff's voltage law

$$\sum_{k=1}^{n-1} m_{k, k+1} + m_{n, 1} = 0 \quad (39)$$

they should satisfy. Our goal is to determine d_k values for $k \in \{1, \dots, n\}$ that provide these line voltage average values.

It is worth to mention that in practice we choose the set of fundamental phase voltages in the form of (38) as the first step, and the set of line voltages we started with in this section is merely a consequence. However, we have chosen to use line voltages as a common approach, since the notion of fundamental phase voltages is not common.

According to (5), line voltages are related to the duty ratio values corresponding phases are operated by such that

$$\begin{aligned} d_1 - d_2 &= m_{1, 2} \\ d_2 - d_3 &= m_{2, 3} \\ &\vdots \\ d_{n-1} - d_n &= m_{n-1, n} \\ d_n - d_1 &= m_{n, 1} \end{aligned} \quad (40)$$

which is a set of n equations over n unknown variables d_k . However, due to (39) only $n-1$ of these equations are independent, and one is redundant. Any of the equations could be chosen as redundant, but let us choose the first to be redundant, to simplify indexing in generalizing the analysis to an arbitrary number of phases. This results in a set of $n-1$ independent equations

$$\begin{aligned} d_2 &= d_1 - m_{1, 2} \\ d_3 &= d_2 - m_{2, 3} \\ &\vdots \\ d_n &= d_{n-1} - m_{n-1, n}. \end{aligned} \quad (41)$$

These $n-1$ equations directly provide $n-1$ duty ratio values depending on the choice of d_1 , such as

$$\begin{aligned} d_2 &= d_1 - m_{1, 2} \\ d_3 &= d_1 - m_{1, 3} \\ &\vdots \\ d_n &= d_1 - m_{1, n} \end{aligned} \quad (42)$$

Thus, the duty ratio d_1 is a free variable and its arbitrary choice implies all other duty ratio values. However, the choice of d_1 cannot be completely arbitrary, since there are physical limits imposed to the duty ratio values.

B. DUTY RATIO LIMITS

According to their definitions, the duty ratio values are limited to

$$0 \leq d_k \leq 1 \quad (43)$$

for $k \in \{1, \dots, n\}$. From (42) for $k \in \{2, \dots, n\}$ this results in

$$0 \leq d_1 - m_{1,k} \leq 1 \quad (44)$$

which results in $n - 1$ constraints over d_1

$$m_{1,k} \leq d_1 \leq 1 + m_{1,k}. \quad (45)$$

In addition, d_1 has its own constraint

$$0 \leq d_1 \leq 1. \quad (46)$$

Chosen value for d_1 , which implies all other duty ratio values, should satisfy all of these n constraints.

C. THE DEGREE OF FREEDOM AND ITS LIMITS

The fact that d_1 should satisfy all of the requirements (45) and (46) results in two limits in the choice of d_1

$$d_{1,min} \leq d_1 \leq d_{1,max} \quad (47)$$

where

$$d_{1,min} = \max(0, m_{1,2}, \dots, m_{1,n}) \quad (48)$$

and

$$d_{1,max} = \min(1, 1 + m_{1,2}, \dots, 1 + m_{1,n}) \quad (49)$$

which could be simplified to

$$d_{1,max} = 1 + \min(0, m_{1,2}, \dots, m_{1,n}) \quad (50)$$

Furthermore, since

$$0 = m_{1,1} \quad (51)$$

the form of d_1 limits could be simplified to

$$d_{1,min} = \max_{1 \leq k \leq n} (m_{1,k}) \quad (52)$$

and

$$d_{1,max} = 1 + \min_{1 \leq k \leq n} (m_{1,k}). \quad (53)$$

Equations (52) and (53) for $d_{1,min}$ and $d_{1,max}$ could be expressed in a slightly different form, having in mind that

$$\begin{aligned} \max_{1 \leq k \leq n} (m_{1,k}) &= \max_{1 \leq k \leq n} (m_1 - m_k) = \\ &= m_1 + \max_{1 \leq k \leq n} (-m_k) = \\ &= m_1 - \min_{1 \leq k \leq n} (m_k) \end{aligned} \quad (54)$$

and

$$\begin{aligned} \min_{1 \leq k \leq n} (m_{1,k}) &= \min_{1 \leq k \leq n} (m_1 - m_k) = \\ &= m_1 + \min_{1 \leq k \leq n} (-m_k) = \\ &= m_1 - \max_{1 \leq k \leq n} (m_k). \end{aligned} \quad (55)$$

This results in

$$d_{1,min} = m_1 - \min_{1 \leq k \leq n} (m_k) \quad (56)$$

and

$$d_{1,max} = m_1 + 1 - \max_{1 \leq k \leq n} (m_k). \quad (57)$$

Expressions (56) and (57) relate the range limits for d_1 to m_1 and values $\min_{1 \leq k \leq n} (m_k)$ and $\max_{1 \leq k \leq n} (m_k)$ that are general to all of the phases. In this manner, the range expressions could straightforwardly be generalized to any phase k just by substituting m_1 with m_k . However, it should be noted that the problem has only one degree of freedom, and that choice of one of the d_k values implies all others according to (42), having in mind $m_{1,k} = m_1 - m_k$.

A consequence of (56) is that for $\min_{1 \leq k \leq n} (m_k) = m_1$, which holds for $\frac{1}{n}$ of the period, $d_{1,min} = 0$, and switching can be avoided. Alternatively, for $\max_{1 \leq k \leq n} (m_k) = m_1$, which applies for $\frac{1}{n}$ of the period again, according to (57) $d_{1,max} = 1$, resulting in the same effect. Thus, by choosing these values for d_1 , the inverter could be operated such that one phase is not switching at any time during the period, while these non-switching phases change every $\frac{1}{n}$ of the period.

Another consequence of (56) and (57) is an expression for the midpoint in the d_1 range

$$\begin{aligned} d_{1,med} &= \frac{1}{2} (d_{1,min} + d_{1,max}) \\ &= \frac{1}{2} + m_1 - \frac{1}{2} \left(\min_{1 \leq k \leq n} (m_k) + \max_{1 \leq k \leq n} (m_k) \right). \end{aligned} \quad (58)$$

In the case of even values of n , for each phase there is its exact opposite in the set, resulting in

$$\min_{1 \leq k \leq n} (m_k) + \max_{1 \leq k \leq n} (m_k) = 0 \quad (59)$$

and

$$d_{1,med} = \frac{1}{2} + m_1 \quad (60)$$

corresponding to the initially assumed values for the pulse width modulation in section II-B. On the other hand, for odd values of n (59) is not satisfied, and the resulting nonzero term contains the zero-sequence AC component [2] which facilitated amplitude gains of space vector modulation [1].

Value of the analysis of d_1 range is in the fact that the choice of d_1 could be used for optimization. Consider a trivial example in which $m = 0$. In that case, $d_{1,min} = 0$, $d_{1,max} = 1$. Desired line voltage average values equal to zero could be achieved applying switching and related losses, or not applying any switching at all. Issues of switching losses, ripple, machine losses, as well as other optimization criteria, could be used to choose an optimal value for d_1 for a given application. Such optimization is performed over one variable, d_1 , within its available range.

D. FEASIBILITY CONSTRAINT

Physical constraints limit the choice of duty ratio values, which resulted in limitations of d_1 given by (47), (56), and (57). The choice of prescribed line voltage values determines whether it is feasible to achieve them under physical duty ratio

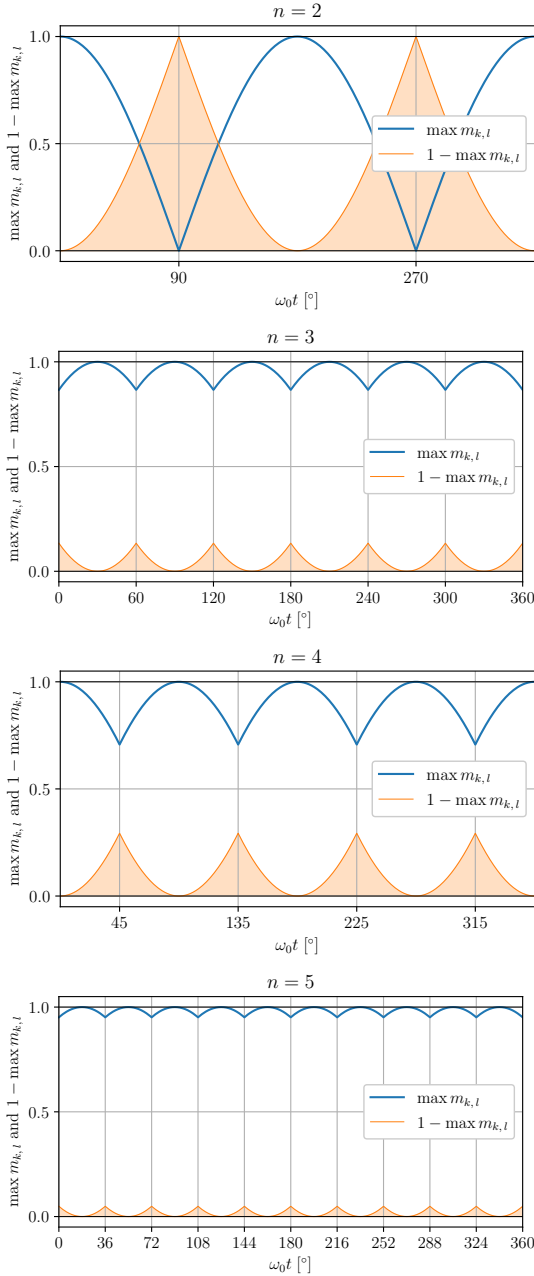


FIGURE 4. Feasibility constraint.

limitations. To have feasible range of d_1 values, which implies all other duty ratio values, it is required to have

$$d_{1,min} \leq d_{1,max}. \quad (61)$$

This, according to (56) and (57), results in

$$\max_{1 \leq k \leq n} (m_k) - \min_{1 \leq k \leq n} (m_k) \leq 1 \quad (62)$$

which can be condensed to

$$\max_{1 \leq k \leq n, 1 \leq l \leq n} (m_{k,l}) \leq 1. \quad (63)$$

In terms of actual voltages, constraint (62) reduces to

$$\max_{1 \leq k \leq n} (v_k) - \min_{1 \leq k \leq n} (v_k) \leq V_{dc}. \quad (64)$$

Physical meaning of the constraint is that the full wave rectified voltage that would result from the considered n phase voltage system should be lower than V_{dc} in order to be feasible to construct it using a voltage source inverter.

To illustrate previous analysis, in Fig. 4 the feasibility constraint (62) is plotted for $n \in \{2, 3, 4, 5\}$ and the normalized phase voltages specified by (38). The fact that plotted waveforms are less or in some points equal to the limiting value could be observed, as well as the waveforms familiar to full wave rectification. Besides, it could be observed that for odd values of the number of phases n , the frequency doubling phenomenon occurs, there are $2n$ periods of the limiting waveform within one line period, while this phenomenon is absent in cases of even values of n , there are only n limiting waveform periods within a line period. Cases of even and odd number of phases differ here, resulting in amplitude gain in the case of the odd number of phases, but also in a reduced range of choice for d_1 , which is a side result.

As a side result, it is worth to mention here that the span for allowable d_1 values according to (56) and (57) is

$$d_{1,max} - d_{1,min} = 1 - \max_{1 \leq k \leq n, 1 \leq l \leq n} (m_{k,l}) \quad (65)$$

which is also plotted in Fig. 4. It can be observed how the frequency doubling phenomenon reduces the allowable range for d_1 in cases of even n .

E. APPLICATION OF THE METHOD, A CASE STUDY

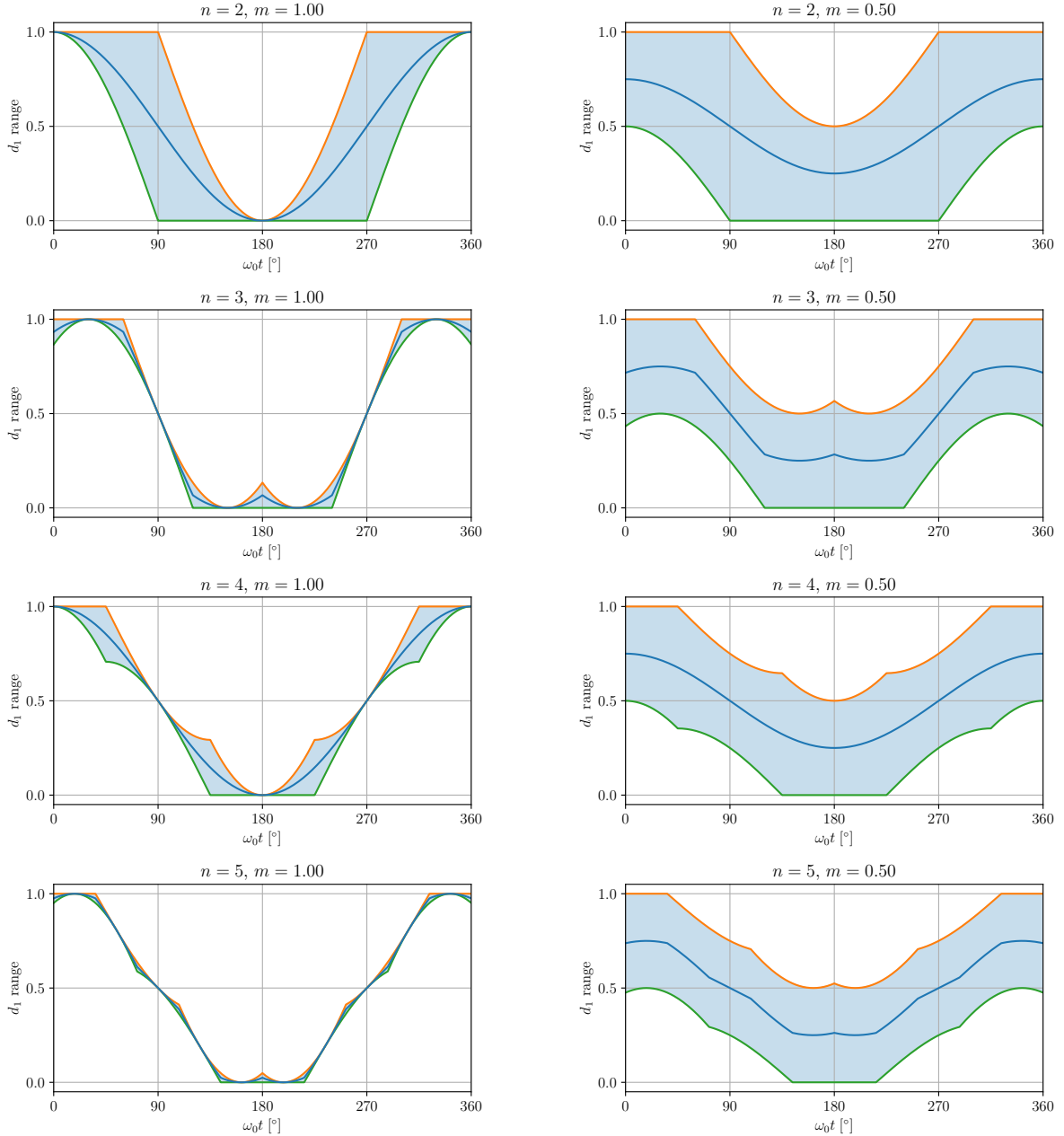
The analysis presented so far resulted in a conclusion that one duty ratio value, for example d_1 , has a degree of freedom to be chosen within a range specified by (56) and (57), while all other duty ratio values are implied by (42).

In the diagrams located in the left column of Fig. 5, range for d_1 is shown for the number of phases ranging from $n = 2$ to $n = 5$ and the modulation index of $m = 1$, corresponding to the maximal amplitude of generated voltages. Values of $d_{1,max}$, $d_{1,min}$, and $d_{1,med}$ are highlighted by thick lines. As predicted, for even values of the number of phases n , the value of $d_{1,med}$ takes sinusoidal waveform of the AC component, which is not a case for odd values of n . Also, for even values of n , the range of d_1 freedom of choice is wider, corresponding to (65) and the waveforms of Fig. 4.

In the diagrams of the right column of Fig. 5, range for d_1 is shown for the modulation index of $m = 0.5$. As expected, reduction of the modulation index widens the range of d_1 , opening space for optimization. Again, even values of n result in sinusoidal AC component of $d_{1,med}$, in contrast to the odd values where the zero-sequence AC components are present. However, these components are getting reduced by increasing the number of phases, as well as the gain in the amplitude.

IV. EXPERIMENTAL RESULTS

In order to prove the concept, an inverter model is built using Raspberry Pi Pico [25]. The model implements the

FIGURE 5. Range of d_1 .

modulation algorithm in the same manner as it would be applied in any inverter, regardless the inverter rated power. For the sake of convenience within the lab constraints, standard microcontroller digital outputs are used to represent the inverter output, providing the same functionality, but at low power, convenient to handle. Such setup is sufficient to verify the algorithm proposed in this paper.

To provide pulse width modulation, standard pulse width modulated outputs are used, and the switching frequency is set to 50 kHz. The lookup table for modulation signals is generated using Python programming language and stored as a Python module such that importing different modules in the

main program results in different modulation strategies. Averaging in the diagrams is provided applying two stage RC filter described in [26], with a double pole at $s_p \approx -2\pi \times 3.4$ kHz. In this manner, the pulse width modulated output of the microcontroller is treated as a digital to analog converter, and the duty ratio is visualized. Frequency of the generated voltages is chosen to be close to 50 Hz, being widely separated from the switching frequency and the filter poles frequency.

Waveforms depicted in Fig. 5 are covered by experimental results such that in diagrams of Fig. 6(a) and 6(d) cases $d_1 = d_{1,min}$ are given for $m = 1$ and $m = 0.5$, in Fig. 6(b) and 6(e) cases $d_1 = d_{1,med}$ are covered, and in Fig. 6(c)

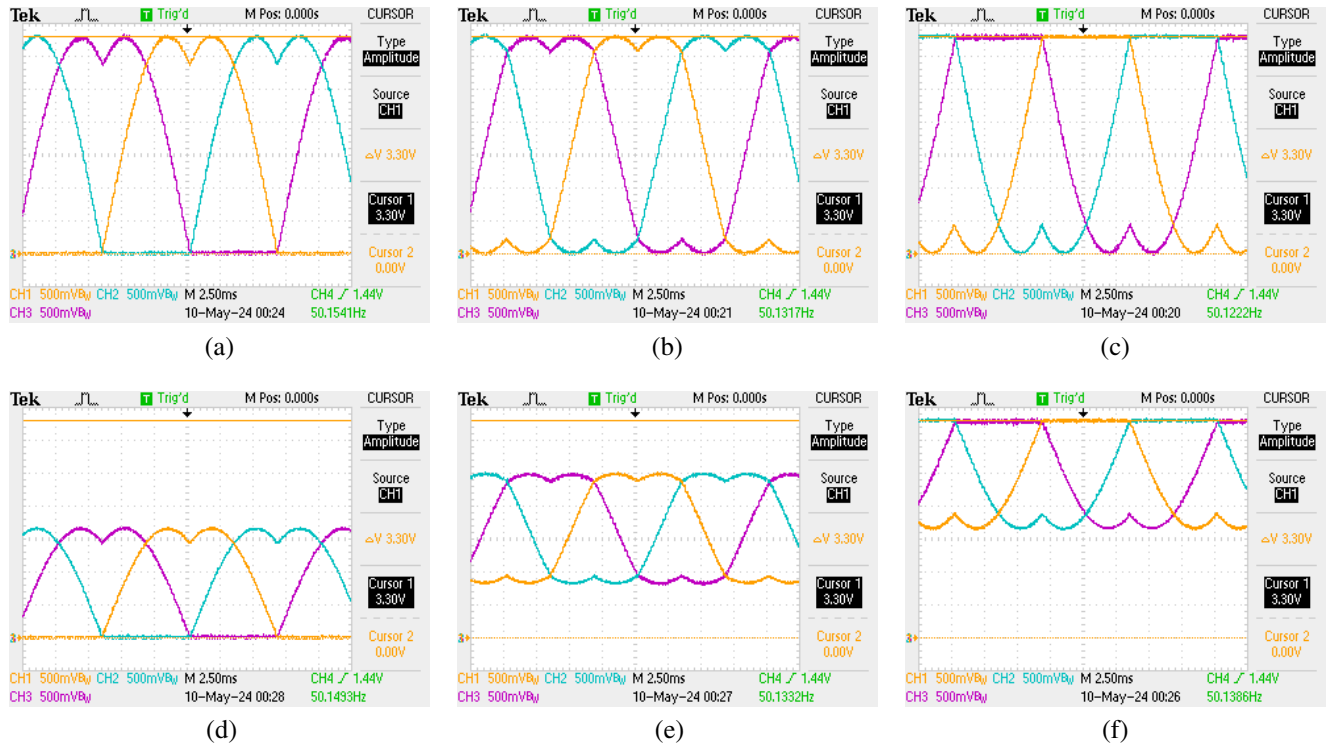


FIGURE 6. Experimental waveforms of $\langle v_1 \rangle$, $\langle v_2 \rangle$, and $\langle v_3 \rangle$, $n = 3$: (a) $m = 1$, $d_1 = d_{1,min}$; (b) $m = 1$, $d_1 = d_{1,med}$; (c) $m = 1$, $d_1 = d_{1,max}$; (d) $m = 0.5$, $d_1 = d_{1,min}$; (e) $m = 0.5$, $d_1 = d_{1,med}$; (f) $m = 0.5$, $d_1 = d_{1,max}$.

and 6(f) cases $d_1 = d_{1,max}$ are covered for the same values of the modulation index. All of the diagrams correspond to theoretical expectations, having the same form for each phase, but shifted for appropriate phase delay.

To relate the waveforms of Fig. 6 to space vectors that correspond to line voltages, according to the notation of [27], trajectory of the averaged space vectors corresponding to the diagrams of Fig. 6(a) to 6(c) are included in Fig. 7, corresponding to overlapping circles with the radii equal to 3.3 V, as well as the the space vector trajectories that correspond to the waveforms of Fig. 6(d) to 6(f), corresponding to circles with the radii close to 1.65 V. Furthermore, trajectories for $m = 0.75$, $m = 0.25$, and $m = 0$ are added, resulting in circles with predicted radii. The space vectors are obtained according to [27], and according to expectations indicate line voltage amplitudes of 3.3 V in the case of $m = 1$, being scaled down linearly according to actual value of m . Regardless the choice of d_1 , in all of the cases the trajectories of the averaged space vectors overlap, and the overlap is complete.

To illustrate instantaneous values of space vectors that correspond to line voltages, experimental data in the same conditions as for Fig. 7 are recorded without filters of [26] and processed according to [27]. The results are presented in Fig. 8, indicating that in all cases averaged space vectors are obtained from seven distinct space vectors that originate from eight switch state combinations.

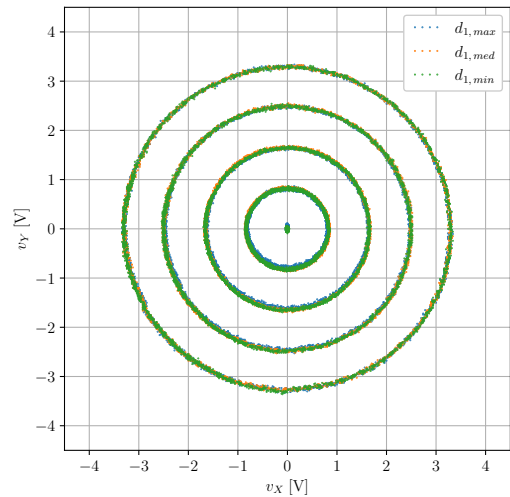


FIGURE 7. Trajectory of the averaged space vector for $m = 1$, $m = 0.75$, $m = 0.5$, $m = 0.25$, and $m = 0$.

V. CONCLUSIONS

In this paper, an algebraic approach to modulation in voltage source inverters with an arbitrary number of phases is proposed. Space vectors were not used in the analysis, since they were not necessary, and the zero-sequence components of the modulating voltages emerged as a mere consequence. It is shown that the problem of determining n duty ratio values d_k that operate n legs of the voltage source inverter does not have a unique solution, having one degree of freedom, but

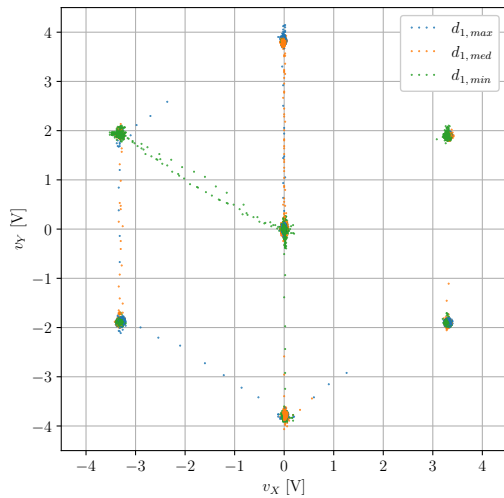


FIGURE 8. Space vectors for $m = 1$, $m = 0.75$, $m = 0.5$, $m = 0.25$, and $m = 0$.

within a limited range. Duty ratio of the first leg, d_1 is chosen to be the degree of freedom, and its choice implies all other duty ratio values. Constraints imposed to d_1 are derived and analyzed, resulting in a range of allowable values. It is shown that the problem of modulating voltage source inverter has significant similarities to its inverse problem, analysis of the full wave n phase rectifier. Feasibility of the modulation is related to the desired line voltages that should always be less or equal to the DC link voltage. To simplify the analysis, notion of a fundamental phase voltage, free of zero-sequence components, is introduced.

Proposed approach clarifies the low-frequency behavior of voltage source inverters and identifies a variable that is a degree of freedom to perform optimization. The approach is general, and it could be applied to any number of phases. Differences in performance for even and odd number of phases are highlighted, indicating that with even number of phases amplitude gain cannot be achieved, but the range of available values of d_1 is higher in comparison to surrounding odd values of the number of phases.

Experimental results are provided being in complete agreement with the presented analysis.

REFERENCES

- [1] H. W. Van Der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulswidth modulator based on voltage space vectors," *IEEE transactions on industry applications*, vol. 24, no. 1, pp. 142–150, 1988.
- [2] P. Pinewski, "Understanding space vector modulation," *EDN*, vol. 41, no. 5A, pp. 45–47, 1996.
- [3] P. J. Perruchoud and P. J. Pinewski, "Power losses for space vector modulation techniques," in *Power Electronics in Transportation*. IEEE, 1996, pp. 167–173.
- [4] R. H. Ahmad, G. G. Karady, T. D. Blake, and P. Pinewski, "Comparison of space vector modulation techniques based on performance indexes and hardware implementation," in *Proceedings of the IECON'97 23rd International Conference on Industrial Electronics, Control, and Instrumentation (Cat. No. 97CH36066)*, vol. 2. IEEE, 1997, pp. 682–687.
- [5] P. J. Pinewski, "Implementing a simple vector controller," in *Proceedings*

- of the 1997 American Control Conference (Cat. No. 97CH36041)*, vol. 1. IEEE, 1997, pp. 262–266.
- [6] J. S. Kim and S. K. Sul, "A novel voltage modulation technique of the space vector pwm," *Chong Hakhoe Nonmunchi (Transactions of the Korean Institute of Electrical Engineers)*, vol. 44, 1995.
- [7] D.-W. Chung, J.-S. Kim, and S.-K. Sul, "Unified voltage modulation technique for real-time three-phase power conversion," *IEEE Transactions on Industry applications*, vol. 34, no. 2, pp. 374–380, 1998.
- [8] J. Holtz, "Pulsewidth modulation—a survey," *IEEE transactions on Industrial Electronics*, vol. 39, no. 5, pp. 410–420, 1992.
- [9] —, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE*, vol. 82, no. 8, pp. 1194–1214, 1994.
- [10] D. Chatterjee, C. Chakraborty, and S. Dalapati, "Pulse-width modulation techniques in two-level voltage source inverters—state of the art and future perspectives," *Power Electronics and Drives*, vol. 8, no. 1, pp. 335–367, 2023.
- [11] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.
- [12] X. Mao, R. Ayyanar, and H. K. Krishnamurthy, "Optimal variable switching frequency scheme for reducing switching loss in single-phase inverters based on time-domain ripple analysis," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 991–1001, 2009.
- [13] O. Onederra, I. Kortabarria, I. M. De Alegria, J. Andreu, and J. I. Gárate, "Three-phase vsi optimal switching loss reduction using variable switching frequency," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6570–6576, 2016.
- [14] S. Albatran, A. S. Allabadi, A. R. Al Khalaileh, and Y. Fu, "Improving the performance of a two-level voltage source inverter in the overmodulation region using adaptive optimal third harmonic injection pulswidth modulation schemes," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 1092–1103, 2020.
- [15] D. Menzi, V. Marugg, T. Langbauer, and J. W. Kolar, "Optimal common-mode voltage injection for phase-modular three-phase pfc rectifiers minimizing energy buffering requirement," *IEEE Open Journal of Power Electronics*, 2023.
- [16] F. Blaabjerg, J. K. Pedersen, and P. Thøgersen, "Improved modulation techniques for pwm-vsi drives," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 1, pp. 87–95, 1997.
- [17] P. Pairedamonchai, S. Suwankawin, and S. Sangwongwanich, "Design and implementation of a hybrid output emi filter for high-frequency common-mode voltage compensation in pwm inverters," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1647–1659, 2009.
- [18] Y. Huang, Y. Xu, W. Zhang, and J. Zou, "Modified single-edge svpwm technique to reduce the switching losses and increase pwm harmonics frequency for three-phase vsis," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 643–10 653, 2020.
- [19] V. Blasko, "Analysis of a hybrid pwm based on modified space-vector and triangle-comparison methods," *IEEE Transactions on industry applications*, vol. 33, no. 3, pp. 756–764, 1997.
- [20] R. J. Kerkman, D. Leggate, B. J. Seibel, and T. M. Rowan, "Operation of pwm voltage source-inverters in the overmodulation region," *IEEE Transactions on Industrial Electronics*, vol. 43, no. 1, pp. 132–141, 1996.
- [21] S. Bolognani and M. Zigliotto, "Novel digital continuous control of svm inverters in the overmodulation range," *IEEE Transactions on Industry Applications*, vol. 33, no. 2, pp. 525–530, 1997.
- [22] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Carrier-based pwm-vsi overmodulation strategies: analysis, comparison, and design," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 674–689, 1998.
- [23] L. Ben-Brahim, "The analysis and compensation of dead-time effects in three phase pwm inverters," in *IECON'98. Proceedings of the 24th Annual Conference of the IEEE Industrial Electronics Society (Cat. No. 98CH36200)*, vol. 2. IEEE, 1998, pp. 792–797.
- [24] U. Abronzini, C. Attaianesi, M. D'Arpino, M. Di Monaco, and G. Tomasso, "Steady-state dead-time compensation in vsi," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5858–5866, 2016.
- [25] D. Dienst, *Raspberry Pi Pico Python SDK: A MicroPython Environment for RP2040 Microcontrollers*. Lulu.com, 2023. [Online]. Available: <https://books.google.rs/books?id=liyxzwEACAAJ>
- [26] P. Pejović, "Output voltage filtering in pulse width modulation based d/a converters," in *2018 International Symposium on Industrial Electronics (INDEL)*. IEEE, 2018, pp. 1–6.
- [27] —, "A simple circuit to visualize space vectors by an oscilloscope," in *2020 International Symposium on Industrial Electronics and Applications (INDEL)*. IEEE, 2020, pp. 1–6.

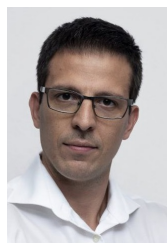


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