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Pulse width modulation for current source inverters with arbitrary number of phases

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Modulation techniques for current source inverters (CSIs) have traditionally been derived from those used for voltage source inverters (VSIs), with space vector modulation (SVM) and pulse width modulation (PWM) being the most popular. Among these, PWM is the preferred choice due to its simplicity and ability to offer the same benefits as SVM, such as increased phase voltage. Ideally, PWM from VSIs could be directly applied to CSIs, but this is not feasible because CSIs require a holistic consideration of all switches on the upper (positive) and lower (negative) rails. In contrast, VSIs allow for per-phase modulation, which enables the straightforward use of a PWM modulator. In this paper, a PWM method tailored specifically for CSIs without any requirements typical for SVM, such as sector identification, is proposed. Using linear algebra, a technique for generating duty cycles averaged over a switching frequency period is derived. These duty cycles are then fed into a specially for CSIs proposed multi-threshold pulse width modulator, which finally produces the gate signals. To validate our method, both simulation and extensive experimental results are presented. The proposed approach is general and applicable to CSIs with any number of phases.

Since the invention of the MOSFET, Voltage Source Inverters (VSIs) have been far more widely used in various applications compared to Current Source Inverters (CSIs). As a result, advancements in modulation and control techniques in power electronics have primarily focused on VSIs. One of the most well-known modulation techniques is Space Vector Modulation (SVM), introduced in[1] for three-phase VSIs. At the time, VSIs used Pulse Width Modulation (PWM) on a per-phase basis[2], and SVM offered approximately 15% more voltage per phase compared to PWM. However, achieving this higher voltage came at a cost—SVM is significantly more complex to implement than PWM. SVM treats the three-phase VSI as a system (rather than considering each phase independently) with multiple switching states—eight valid states in the case of a three-phase VSI. Each state defines a vector, and by applying these vectors, the VSI can deliver a desired voltage to the three-phase load, where the average over one switching period equals the reference voltage vector. Although SVM provided a voltage advantage, it was computationally more demanding and more challenging to implement. This situation persisted until approximately[3], when it was discovered that the same voltage increase could be achieved using PWM by optimizing its degree of freedom—the common-mode voltage—such as by selecting it as a third harmonic. From that point on, PWM became the dominant modulation technique, especially for microcontroller implementations.

The development of modulation techniques for CSIs did not follow a distinct path but was instead derived from VSI modulation techniques, many based on the VSI-CSI duality[4,5]. Consequently, some methods attempt to directly map VSI gate signals to CSI gate signals[6]. Unlike VSIs, CSIs do not operate on a per-phase basis; instead, the switches connected to the upper (positive) rail are treated as a unified entity, as the DC link current flow must always be maintained. Similarly, switches near the lower (negative) rail are also considered as a single entity. Due to this, PWM techniques, which rely on per-phase operation, cannot be directly applied to CSIs. As a result, SVM was adapted for CSI analysis as early as[7], and it has remained in use for CSIs ever since, often leading to complex space vector visualizations[8–14]. In particular, multiphase CSIs, frequently incorporating a fourth bridge leg, also employ SVM, resulting in even more intricate modulation schemes[8–10,15–18]. Given that CSIs are not inherently compatible with PWM, they have continued to rely on SVM. Although there have been attempts to implement PWM for CSIs, these efforts have not yielded a pure PWM approach, where one would only compare a duty cycle value with a carrier signal. Instead, they still retain typical SVM requirements, such as sector identification[19–21]. In addition, all of these methods are limited to three-phase or four-phase CSIs. There is currently no method in the literature that provides a general modulation solution for a CSI with an arbitrary

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number of phases. Therefore, the method proposed in this paper offers both simplicity and generality for n-phase CSIs, which is what sets it apart from existing CSI modulation methods in the literature.

In essence, the modulation process must generate gate signals that simply indicate when a switch is on or off. For VSIs, this is easily accomplished using PWM, which offers all the benefits of SVM—such as increased voltage amplitude—while maintaining simplicity and ease of implementation[3]. However, as discussed earlier, no such straightforward method exists for CSIs.

This paper addresses that gap by proposing a pure PWM technique for CSIs. Our approach directly generates gate signals from current references without the need for sector identification or other SVM-like requirements. To achieve this, the average duty cycles are computed first, which are then processed by our proposed multi-threshold pulse width modulator—a novel solution that enables pure PWM modulation for CSIs. The average duty cycles are obtained using only linear algebra, without any space vectors. A similar approach applied for VSIs can be found in[22], being very simple to use and general, i.e., it works for an arbitrary number of phases n.

The proposed CSI modulation method is general and applicable to an n-phase CSI, whose schematic is depicted in Fig. 1 (where only the first and the n-th bridge legs are shown). Therefore, the proposed method can be implemented in any CSI inverter application, such as CSIs used in drive systems for powering electrical machines or in photovoltaic systems interfacing with single-phase or three-phase power grids. While this paper focuses on CSIs, the method is equally applicable to current source rectifiers. It is important to note that $n \geq 2$. The inverter is powered by a DC link current source I_{dc}, and the following analysis assumes that this current may either vary over time or remain constant—the modulation works in either case. The inverter consists of $2n$ unidirectional switches, grouped into upper switches S_{u1} to S_{un}, and lower switches S_{l1} to S_{ln}. The primary objective of this paper is to determine the average duty ratio values d_{uk} and d_{lk} for $k \in \{1, \ldots n\}$. These values are then applied to the proposed multi-threshold modulator, which generates the switching signals that control S_{uk} and S_{lk}, ultimately ensuring the desired average values for the inverter output currents $\langle i_1 \rangle$ to $\langle i_n \rangle$.

Essential constraint in operating the switches is that only one switch from the upper switches group, S_{uk}, conducts at any time instant, as well as one of the switches in the lower switches group, S_{lk}. At least one switch per group is needed to provide the DC-link current flow, while the number reduces to exactly one switch per group by unidirectional switches, depicted with diodes connected in series to controlled switches in the circuit diagram of Fig. 1, utilized to avoid interphase short-circuiting at the load side.

Requirements, equations, and constraints

Averages of the phase currents

Averages of the phase currents over a switching period T_s in the considered inverter are

$$\langle i_k \rangle = I_{dc} \, (d_{uk} - d_{lk}) \, . \tag{1}$$

The average phase current value, $\langle i_k \rangle$, is the desired quantity, which is achieved by applying the appropriate duty cycles.

Flow of the DC-link current, duty ratio constraints

To provide the DC-link current flow through the upper switches, at each time point exactly one of these switches should be on. This results in the duty ratio constraint for the upper switches

$$\sum_{k=1}^{n} d_{uk} = 1. \tag{2}$$

The same applies for the lower switches, resulting in

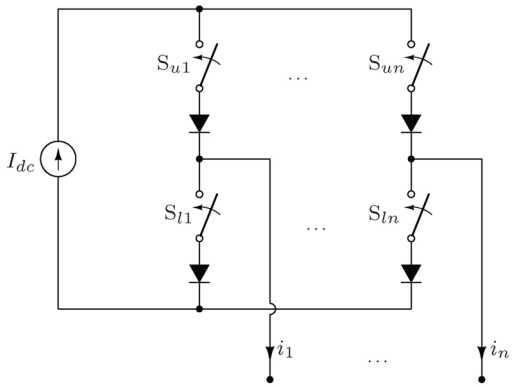

Fig. 1. Schematic diagram of an n-phase Current Source Inverter (CSI). The upper switches are denoted by the subscript u, while the lower switches are indicated by the subscript l.

$$\sum_{k=1}^{n} d_{lk} = 1. \tag{3}$$

Duty ratio limitations

Duty ratio values are always required to be within the range from 0 to 1,

$$0 \leq d_{uk} \leq 1 \quad \text{and} \quad 0 \leq d_{lk} \leq 1. \tag{4}$$

As a consequence of the lower limit in (4) ($0 \leq$), as well as the constraints (2) and (3), all of the upper limits of (4) (≤ 1) are implicitly satisfied, and the lower limits should be the ones taken care of.

Sum of the phase currents

Since the load is assumed to be connected to *n* output phases of the inverter only, Kirchhoff's current law implies that sum of the phase currents equals zero

$$\sum_{k=1}^{n} i_k = 0. \tag{5}$$

Averaging the above equation over the switching period, the same is derived for the averages of the phase currents

$$\sum_{k=1}^{n} \langle i_k \rangle = 0. \tag{6}$$

Substituting (1) in (6), and applying the DC-link flow constraints (2) and (3), the following expressions are obtained

$$\sum_{k=1}^{n} I_{dc}\ (d_{uk} - d_{lk}) = I_{dc} \left(\sum_{k=1}^{n} d_{uk} - \sum_{k=1}^{n} d_{lk} \right) = I_{dc}\ (1-1) = 0, \tag{7}$$

meaning that the sum of the phase currents constraint is implicitly satisfied by the DC-link current flow constraints. However, the form of (6) is convenient and it will be used in subsequent derivations.

Excess duty ratio and minimal realization

For an inverter leg duty ratio values d_{u0k} and d_{l0k} increase in both of the duty ratio values for Δd_k results in

$$\langle i_k \rangle = I_{dc}\ (d_{u0k} - d_{l0k}) = I_{dc}\ ((d_{u0k} + \Delta d_k) - (d_{l0k} + \Delta d_k)) \tag{8}$$

meaning that the average phase current remains the same. Not to affect the lower duty ratio limit for d_{u0k} and d_{l0k}, let assume that

$$\Delta d_k \geq 0. \tag{9}$$

For $d_{u0k} + \Delta d_k$ and $d_{l0k} + \Delta d_k$ to be new duty ratio values, they should satisfy

$$0 \leq d_{u0k} + \Delta d_k \leq 1 \quad \text{and} \quad 0 \leq d_{l0k} + \Delta d_k \leq 1, \tag{10}$$

where the lower limit is implicitly satisfied by (9) as d_{u0k} and d_{l0k} are already the duty ratio functions, and the upper limit remains to be satisfied.

Minimal realization is defined by d_{u0k} and d_{l0k} values which satisfy that either $d_{u0k} = 0$ or $d_{l0k} = 0$. Therefore, from (8), if $\langle i_k \rangle$ is positive, $d_{l0k} = 0$, and other way around, if $\langle i_k \rangle$ is negative, $d_{u0k} = 0$. In the case of nonminimal realization, $d_{uk} > 0$ and $d_{lk} > 0$, the corresponding minimal realization is obtained by

$$d_{u0k} = d_{uk} - \min\left(d_{uk},\, d_{lk}\right) \quad \text{and} \quad d_{l0k} = d_{lk} - \min\left(d_{uk},\, d_{lk}\right), \tag{11}$$

where the excess duty ratio at phase *k* is then given by

$$\Delta d_k = \min\left(d_{uk},\, d_{lk}\right). \tag{12}$$

Therefore, minimal realization d_{u0k} and d_{l0k} satisfy the minimal condition, which is the average of the output currents (8), but not necessarily satisfy the flow equations (2) and (3).

Summary of the problem

Our goal in this paper is to determine the duty ratio values d_{uk} and d_{lk} that provide required values of averaged phase currents $\langle i_k \rangle$ and satisfy constraints (2), (3), and (4). The problem reduces to a linear algebra problem of a set of linear equations that can be summarized as follows:

1. There are $2\ n$ unknown variables, d_{uk} and d_{lk} for $k \in \{1, \ldots n\}$.
2. There are two constraints, imposed by the requirement of the DC-link current flow, $\sum_{k=1}^{n} d_{uk} = 1$ and $\sum_{k=1}^{n} d_{lk} = 1$, both of which are linear equations.
3. There are n equations that specify $\langle i_k \rangle$, as determined by (1), all of them are linear equations over d_{uk} and d_{lk}.
4. One equation from the previous group of equations over $\langle i_k \rangle$ is redundant since $\sum_{k=1}^{n} \langle i_k \rangle = 0$.

Counting the equations and the unknown variables, it is concluded that the system of equations does not have a unique solution since there are

$$n_{df} = 2\,n - 2 - (n-1) = n - 1 \tag{13}$$

degrees of freedom, i.e. variables that can be chosen arbitrarily, but within a certain range to satisfy (4).

Obtaining the duty ratio values

Let us consider a set of average values of a current source inverter output currents $\langle i_k \rangle$ for $k \in \{1, \ldots n\}$ that satisfies constraint (6), and which obtained from a DC source I_{dc} where it is assumed $I_{dc} > 0$. Using the Heaviside step function

$$\mathrm{h}\,(x) = \begin{cases} 0 & x < 0 \\ \frac{1}{2} & x = 0 \\ 1 & x > 0 \end{cases} \tag{14}$$

to provide compact notation, these average currents could be decomposed in their positive and negative parts

$$\langle i_k \rangle_+ = \langle i_k \rangle\ \mathrm{h}\,(\langle i_k \rangle) \quad \text{and} \quad \langle i_k \rangle_- = -\langle i_k \rangle\ \mathrm{h}\,(-\langle i_k \rangle)\,, \tag{15}$$

resulting in

$$\langle i_k \rangle = \langle i_k \rangle_+ - \langle i_k \rangle_- \tag{16}$$

where both of the values (15) are nonnegative.

In practice, application of the Heaviside function is not computationally efficient, and it is used here just to provide compact notation. Instead, two distinct branching based functions would be used to separate positive and negative parts.

According to (1) and (8), minimal realizations of the duty ratio values are

$$d_{u0k} = \frac{\langle i_k \rangle_+}{I_{dc}} \quad \text{and} \quad d_{l0k} = \frac{\langle i_k \rangle_-}{I_{dc}} \tag{17}$$

where at least one of them equals zero. It should be noted that according to (6), (16), and (17)

$$\sum_{k=1}^{n} d_{u0k} = \sum_{k=1}^{n} d_{l0k}. \tag{18}$$

Feasibility constraint for the given problem is

$$\sum_{k=1}^{n} d_{u0k} \leq 1 \tag{19}$$

and the inequality applies in the same form to d_{l0k} according to (18), making it redundant. To satisfy constraints for the flow of the DC-link current (2) and (3), total excess duty ratio is defined as

$$\Delta d = 1 - \sum_{k=0}^{n} d_{u0k} \tag{20}$$

and in the case the required current average values $\langle i_k \rangle$ are feasible for a given value of I_{dc}, it has a nonnegative value

$$\Delta d \geq 0. \tag{21}$$

To satisfy (2) and (3) the excess duty ratio values Δd_k should satisfy

$$\sum_{k=1}^{n} \Delta d_k = \Delta d. \tag{22}$$

To fulfill this requirement, there are n unknown variables, Δd_k, and one constraint (22), which corresponds in $n-1$ degrees of freedom (13) to chose Δd_k values. These degrees of freedom may be used to perform optimization. One solution for a given problem is to share Δd to Δd_k values equally

$$\Delta d_k = \frac{1}{n}\,\Delta d \tag{23}$$

which may be used just to provide actual d_{uk} and d_{lk} values without any optimization, resulting in

$$d_{uk} = d_{u0k} + \frac{1}{n}\,\Delta d \quad \text{and} \quad d_{lk} = d_{l0k} + \frac{1}{n}\,\Delta d, \tag{24}$$

where d_{u0k}, d_{l0k} and Δd are defined by (17) and (20).

In this approach, the CSI modulation process is resolved for the general case, where the phase currents $\langle i_k \rangle$ are not required to be sinusoidal. The duty cycle values are calculated to match any desired average value of the phase currents, while the excess duty cycle is determined to ensure the continuous flow of the DC link current.

The case of sinusoidal symmetrical polyphase currents

A case of special interest in practice is the case of symmetrical polyphase currents with the average values

$$\langle i_k \rangle\,(\omega_0 t) = I_m\,\cos\left(\omega_0 t - (k-1)\,\frac{2\,\pi}{n}\right) \tag{25}$$

where $k \in \{1,\,\ldots\,n\}$. It should be noted that $\langle i_k \rangle = \langle i_k \rangle\,(\omega_0 t)$ is a function of time t, or equivalently of the phase angle $\omega_0 t$, which introduces notions such as the waveform period T_0, frequency $f_0 = 1/T_0$, angular frequency $\omega_0 = 2\,\pi\,f_0$, and amplitude I_m. In comparison to the general case from the previous section, where generated currents are analyzed within the scope of one switching period, in this case, the scope is expanded to one line cycle period, i.e., the waveform period. Further development of this analysis would yield a maximal amplitude that can be achieved and a modulation index that scales down the achievable waveforms.

According to (1),

$$I_{dc}\;(d_{uk} - d_{lk}) = I_m\,\cos\left(\omega_0 t - (k-1)\,\frac{2\,\pi}{n}\right) \tag{26}$$

and the aim that the duty ratio functions d_{uk} and d_{lk} over a line period are functions of $\omega_0 t$. In this aim, three questions arise:

1. How big $I_{m\,max} = \max\,(I_m)$ that can be realized under constraints (4) is?
2. How the duty ratio functions d_{uk} and d_{lk} depend on the phase current amplitude I_m for $0 \le I_m \le I_{m\,max}$?
3. How the value of Δd depends on the phase current amplitude I_m for $0 \le I_m \le I_{m\,max}$?

Minimal realizations of the phase currents

First, let us determine the minimal realizations. For the notational convenience, let us define the phase angle variable for the k^{th} phase as

$$\varphi_k\,(\omega_0 t) = \omega_0 t - (k-1)\,\frac{2\,\pi}{n} \tag{27}$$

resulting in

$$\langle i_k \rangle\,(\omega_0 t) = I_m\,\cos\left(\varphi_k\,(\omega_0 t)\right). \tag{28}$$

Next, let us define two auxiliary functions

$$u_k\,(\omega_0 t) = \cos\left(\varphi_k\,(\omega_0 t)\right)\;\mathrm{h}\left(\cos\left(\varphi_k\,(\omega_0 t)\right)\right) \tag{29}$$

and

$$l_k\,(\omega_0 t) = -\cos\left(\varphi_k\,(\omega_0 t)\right)\;\mathrm{h}\left(-\cos\left(\varphi_k\,(\omega_0 t)\right)\right) \tag{30}$$

in the manner of (15), again as a notational convenience. Functions $u_k\,(\omega_0 t)$ and $l_k\,(\omega_0 t)$ satisfy

$$0 \le u_k\,(\omega_0 t) \le 1 \tag{31}$$

and

$$0 \le l_k\,(\omega_0 t) \le 1 \tag{32}$$

the same constraints as imposed to duty ratio values. It should also be noted that

$$\cos\left(\varphi_k\left(\omega_0 t\right)\right) = u_k\left(\omega_0 t\right) - l_k\left(\omega_0 t\right) \tag{33}$$

which is decomposition of the cosine function to minimal positive values.

Maximum of the phase current average value amplitude that can be obtained applying the analyzed current source inverter is according to (1) linearly dependent on the DC-link current

$$I_{m\,max} = a\, I_{dc} \tag{34}$$

where a is the amplitude parameter, dependent on the number of phases n.

From (1), (33), and (34), the minimal realization is

$$I_{dc}\ \left(d_{u0k}\left(\omega_0 t\right) - d_{l0k}\left(\omega_0 t\right)\right) = a\, I_{dc}\ \left(u_k\left(\omega_0 t\right) - l_k\left(\omega_0 t\right)\right) \tag{35}$$

which is satisfied for

$$d_{u0k}\left(\omega_0 t\right) = a\, u_k\left(\omega_0 t\right) \quad \text{and} \quad d_{l0k}\left(\omega_0 t\right) = a\, l_k\left(\omega_0 t\right). \tag{36}$$

According to (6), (25), and (33), there is

$$\sum_{k=1}^{n} \cos\left(\varphi_k\left(\omega_0 t\right)\right) = \sum_{k=1}^{n} u_k\left(\omega_0 t\right) - \sum_{k=1}^{n} l_k\left(\omega_0 t\right) = 0 \tag{37}$$

resulting in

$$\sum_{k=1}^{n} u_k\left(\omega_0 t\right) = \sum_{k=1}^{n} l_k\left(\omega_0 t\right) \tag{38}$$

which is an important property to be used in the subsequent derivation.

Maximum of the phase current amplitude

Maximum of the phase current amplitude that can be obtained by the analyzed inverter is limited by the duty ratio constraints (2) and (3). It should be noted here that $\sum_{k=1}^{n} u_k = \sum_{k=1}^{n} l_k$ are not constant, thus neither are $\sum_{k=1}^{n} d_{u0k}$ and $\sum_{k=1}^{n} d_{l0k}$, regardless the fact that with increasing of the number of phases n these values are getting closer to a constant value. Since d_{u0k} and d_{l0k} correspond to minimal realization, corresponding actual duty ratio values

$$d_{uk}\left(\omega_0 t\right) = d_{u0k}\left(\omega_0 t\right) + \Delta d_k\left(\omega_0 t\right) \quad \text{and} \quad d_{lk}\left(\omega_0 t\right) = d_{l0k}\left(\omega_0 t\right) + \Delta d_k\left(\omega_0 t\right), \tag{39}$$

should be increased over the minimal realization for Δd_k to make the sums equal to one. Since $\Delta d_k \geq 0$, the minimal realization duty ratio values should satisfy

$$\sum_{k=1}^{n} d_{u0k}\left(\omega_0 t\right) \leq 1 \quad \text{and} \quad \sum_{k=1}^{n} d_{l0k}\left(\omega_0 t\right) \leq 1, \tag{40}$$

which is the same constraint as a consequence of (36), and (38). So, let us focus on (40) as sufficient, which results in

$$a \sum_{k=1}^{n} u_k\left(\omega_0 t\right) \leq 1. \tag{41}$$

At this point, it is convenient to define an auxiliary function $w\left(\omega_0 t\right)$ as

$$w\left(\omega_0 t\right) = \sum_{k=1}^{n} u_k\left(\omega_0 t\right). \tag{42}$$

This leads to the definition of w_{max} as

$$w_{max} = \max_{0 \leq \omega_0 t \leq 2\,\pi} w\left(\omega_0 t\right) \tag{43}$$

and from the maximum amplitude constraint (41)

$$a\, w_{max} = 1 \quad \text{it is finally obtained} \quad a = \frac{1}{w_{max}}, \tag{44}$$

which according to (34) determines maximum of the phase current amplitude. This also limits the minimal realization duty ratio functions to $d_{u0k} \leq a$ and $d_{l0k} \leq a$.

The value of a depends on the number of phases n, making it a function of the inverter number of phases, $a\,(n)$. Numerically computed values of $a\,(n)$ for $2 \leq n \leq 12$ are given in Fig. 2. For the single-phase inverter, $n = 2$, as well as for the three-phase inverter, $n = 3$, maximal amplitude of the phase currents equals to the DC-link current. However, for higher number of phases the maximal amplitude is lower than the DC-link current according to the $a\,(n)$ function that asymptotically approaches $I_m = \frac{\pi}{n}\, I_{dc}$ as $n \to \infty$, since I_{dc} approaches a sum of the output current of n half-wave rectifiers interleaved such that ripple of the sum over a line period is getting negligible.

Variable amplitude of the phase currents

After the minimal realization of the duty ratio functions is determined, as well as the maximum of the phase currents, the next task is to determine minimal realizations of the duty ratio functions for arbitrary amplitude of the phase currents

$$I_m = m\, I_{m\,max} = m\, a\, I_{dc} \tag{45}$$

where m is the modulation index

$$0 \leq m \leq 1 \tag{46}$$

which scales down the waveforms. Since

$$\langle i_k \rangle\,(\omega_0 t) = m\, I_{m\,max}\, \cos\left(\varphi_k\,(\omega_0 t)\right) = m\, a\, I_{dc}\,\left(u_k\,(\omega_0 t) - l_k\,(\omega_0 t)\right) \tag{47}$$

the minimal realization duty ratios in the case of the arbitrary amplitude are

$$d_{u0k}\,(\omega_0 t) = m\, a\, u_k\,(\omega_0 t) \quad \text{and} \quad d_{l0k}\,(\omega_0 t) = m\, a\, l_k\,(\omega_0 t)\,. \tag{48}$$

It should also be noted here that according to (18) sum of the upper duty ratio functions equals the sum of the lower duty ratio functions, which are functions of the phase angle now

$$\sum_{k=1}^{n} d_{u0k}\,(\omega_0 t) = \sum_{k=1}^{n} d_{l0k}\,(\omega_0 t)\,. \tag{49}$$

In minimal realizations, these sums are not constant, neither always equal to one.

Excess of the duty ratio

To satisfy the requirements of (2) and (3), duty ratio values d_{uk} and d_{lk} should be increased over their minimal realization values d_{u0k} and d_{l0k} for Δd_k according to (8). The total extra duty ratio (20) Δd now becomes a function of the phase angle

$$\Delta d\,(\omega_0 t) = \sum_{k=1}^{n} \Delta d_k\,(\omega_0 t) \tag{50}$$

the same as particular duty ratio excess values Δd_k. According to (20)

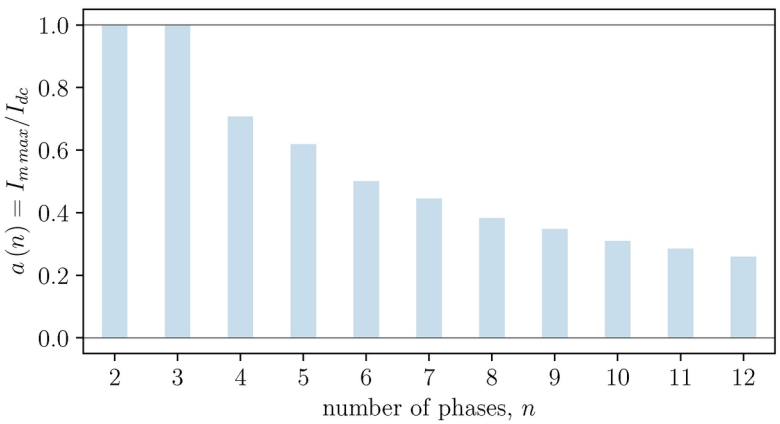

Fig. 2. Maximum amplitude parameter as it depends on the number of phases, $a\,(n)$.

$$\Delta d\left(\omega_0 t\right) = 1 - \sum_{k=1}^{n} d_{u0k}\left(\omega_0 t\right) \tag{51}$$

and it should be distributed into n possibly different Δd_k values, which brings $n-1$ degree of freedom in our problem of obtaining the duty ratio values, again.

Since according to (42)

$$\sum_{k=1}^{n} d_{u0k}\left(\omega_0 t\right) = m\, a \sum_{k=1}^{n} u_k\left(\omega_0 t\right) = m\, a\, w\left(\omega_0 t\right) \tag{52}$$

the total excess duty ratio is obtained as

$$\Delta d\left(\omega_0 t\right) = 1 - m\, a\, w\left(\omega_0 t\right) \tag{53}$$

and depends on the modulation index. Again, one solution is to spread Δd over Δd_k equally (23)

$$\Delta d_k\left(\omega_0 t\right) = \frac{1}{n}\,\Delta d\left(\omega_0 t\right) = \frac{1}{n}\,\left(1 - m\, a\, w\left(\omega_0 t\right)\right). \tag{54}$$

This analysis is just an application of the method described in the previous section to the case of symmetrical polyphase currents, which introduces notions of the maximum amplitude parameter a and the modulation index m by observing the waveforms on the line period level that is wider than the switching period level used in the previous section where arbitrary waveforms are assumed.

Scaling

Finally, to provide a scalable amplitude of the generated currents, duty ratio values od (48) with the excess duty ratio given by (54) should be joined together to obtain the final duty ratio values

$$d_{uk}\left(\omega_0 t\right) = \frac{1}{n} + a\left(u_k\left(\omega_0 t\right) - \frac{w\left(\omega_0 t\right)}{n}\right) m \quad \text{and} \quad d_{lk}\left(\omega_0 t\right) = \frac{1}{n} + a\left(l_k\left(\omega_0 t\right) - \frac{w\left(\omega_0 t\right)}{n}\right) m. \tag{55}$$

In these expressions, the first term is a constant, while the second term is a function of time, a pattern, scaled with the value of m. Sampled values of the pattern would be stored in a lookup table. To reduce the storage space, symmetry properties of the patterns might be used. In the case of symmetrical three-phase currents, such storage space reduction is to one quarter of the original storage space.

Examples

To illustrate the modulation technique, in the left column of Fig. 3 waveforms of the minimal realization duty ratios d_{u01} and d_{l01} are presented, as well as the total excess duty ratio function Δd for the inverters ranging from $n = 2$ (which is a single phase inverter) to $n = 5$ phases, with the modulation index $m = 1$ corresponding to the maximal amplitude, while in the right column of Fig. 3 the same values are presented for $m = 0.5$, that corresponds to one half of the maximal amplitude. The duty ratio values d_{u0k} and d_{l0k} for phases other than $k = 1$ are just phase shifted right for $(k-1)\,\frac{2\,\pi}{n}$.

Analyzing the diagrams of Fig. 3, as well as the diagrams that correspond to higher number of phases not presented here, it is concluded that Δd variation is higher for even values of n in comparison to the surrounding odd phase number values $n-1$ and $n+1$. Also, the waveform of Δd is periodic with T_0/n for even number of phases n, where T_0 is the line period, while it is periodic with $T_0/\left(2\,n\right)$ for odd number of phases, doubling the frequency. Furthermore, the span covered by the excess duty ratio Δd is higher for lower modulation index values, as predicted by (53), reaching its maximum for $m = 0$. Increasing the number of phases reduces variation in Δd over the line period.

To illustrate actual duty ratio values, waveforms of d_{u1} and d_{l1} are presented in the left column of Fig. 4, for the modulation index $m = 1$, corresponding to the maximal amplitude, and for the number of phases varying from $n = 2$ to $n = 5$, again. The line corresponds to equal sharing of the total excess duty ratio according to (54), while the shaded area represents values that can be reached by different algorithms of sharing the excess duty ratio. Corresponding diagrams for the modulation index of $m = 0.5$ are presented in the right column of Fig. 4, indicating lower duty ratio values and wider span of achievable duty ratio values.

Generalization to arbitrary periodic waveforms

The analysis of periodic waveforms of generated currents presented up to this point covers symmetrical sinusoidal polyphase currents. To preserve notions of amplitude I_m, maximal amplitude parameter a, and the modulation index m, the method could easily be generalized to arbitrary periodic waveforms of the output current averaged values that satisfy constraint (6). This generalization might be of interest to cover unbalanced sinusoidal waveforms[8–10,16], overmodulation, and any other periodic waveforms of generated currents.

The first step in this generalization is to generalize the notion of amplitude I_m, and it is defined here as a maximum absolute value of output current switching frequency average values as

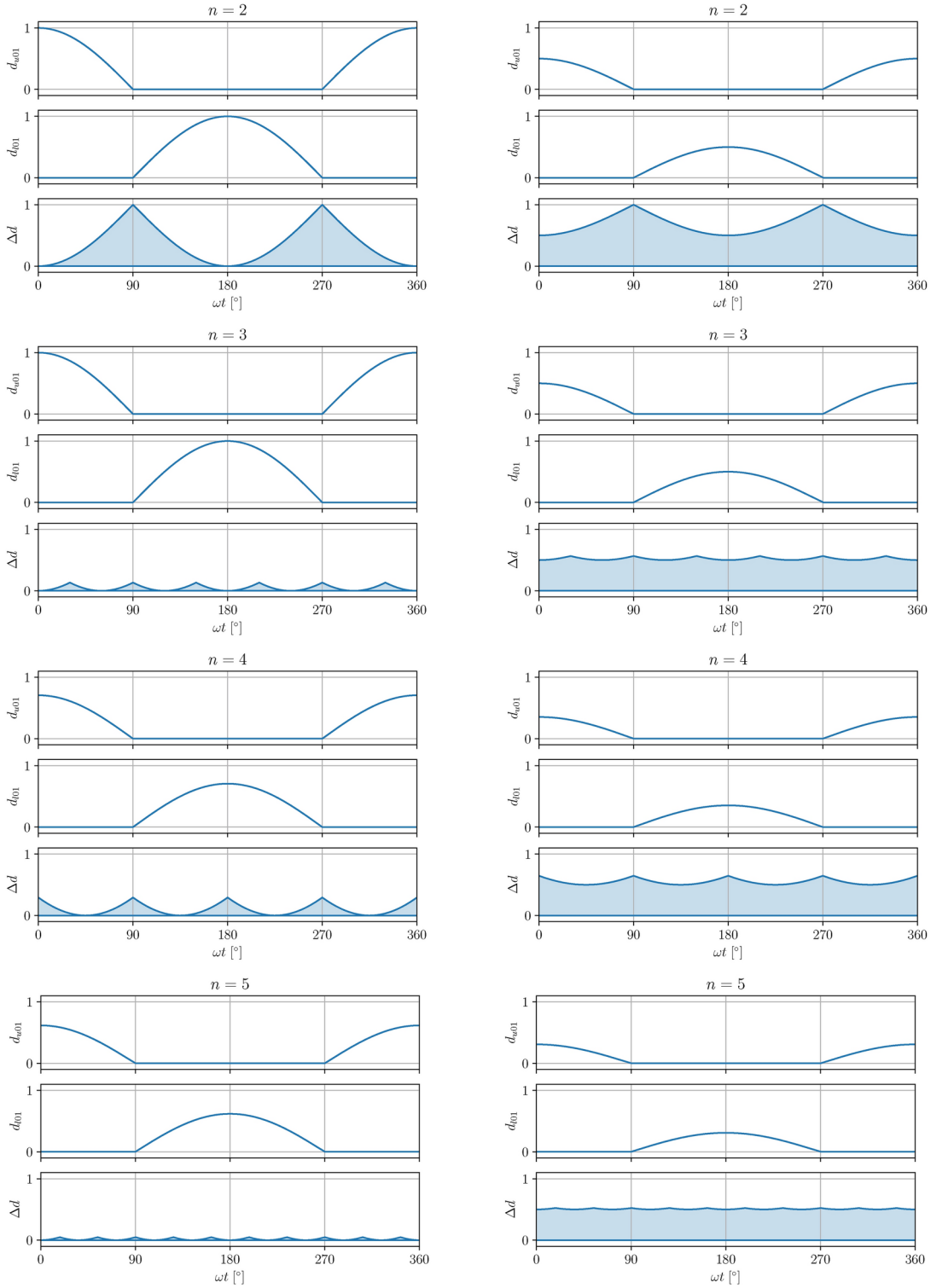

Fig. 3. Duty ratio functions d_{u01},d_{l01}, and Δd : left column, $m = 1$; right column, $m = 0.5$.

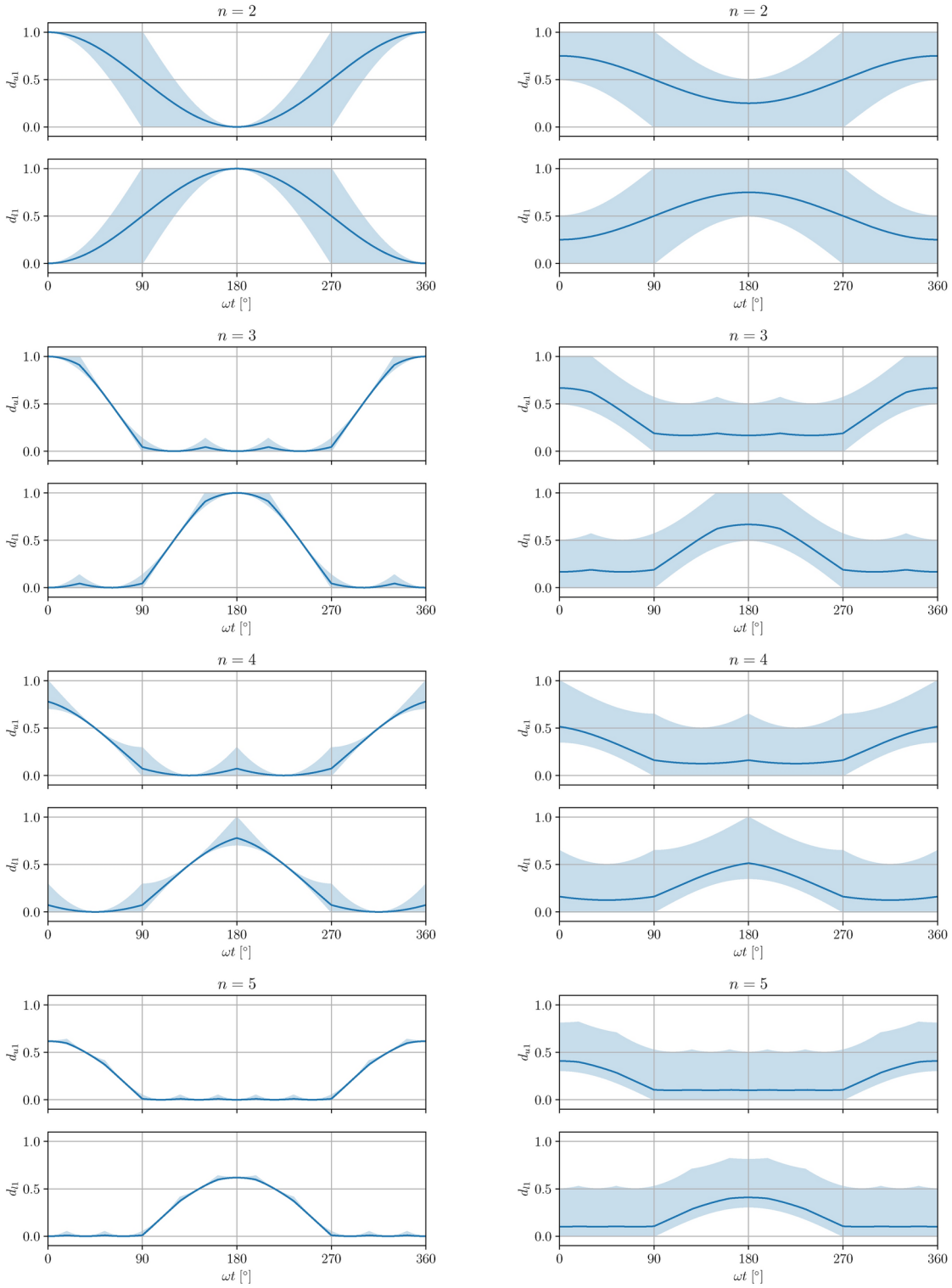

Fig. 4. Duty ratio functions d_{u1} and d_{l1} : left column, $m = 1$; right column, $m = 0.5$.

$$I_m = \max_{1 \le k \le n} \left(\max_{0 \le t \le T_0} \left(\left| \langle i_k \rangle (t) \right| \right) \right). \tag{56}$$

This choice affects the definitions of auxiliary functions (29) and (30), redefining them as

$$u_k = \frac{\langle i_k \rangle}{I_m} \, \mathrm{h} \left(\frac{\langle i_k \rangle}{I_m} \right) \quad \text{and} \quad l_k = -\frac{\langle i_k \rangle}{I_m} \, \mathrm{h} \left(-\frac{\langle i_k \rangle}{I_m} \right), \tag{57}$$

which reduces to (29) and (30) in the symmetrical polyphase sinusoidal case. This choice of I_m provides that values of u_k and l_k satisfy (31) and (32), making it possible for $I_{dc} \ge I_m$ to realize each of $\langle i_k \rangle$ values according to (1) as a single current, regardless of other currents.

After the definitions of u_k and l_k are generalized, the analysis proceeds in the same way, with the same definitions of w (42), w_{max} (43), and a (44), resulting in the value of a that makes realization of all $\langle i_k \rangle$ values for $k \in \{1, \ldots n\}$ from I_{dc} feasible, modeling their interaction.

Finally, minimal realizations d_{u0k} and d_{l0k} are obtained according to (48), resulting in the total excess duty ratio Δd of (53), which is then shared to particular excess duty ratio values Δd_k.

Resulting duty ratio waveforms would be different than presented in Figs. 3 and 4, depending on the required currents, but the analysis would be the same.

In this manner, notion of the amplitude is generalized to (56), affecting notions of the maximal amplitude parameter (44) and the modulation index (45) for an arbitrary set of periodic phase current waveforms. It is worth to underline here that the amplitude I_m is chosen to be able to generate each of the $\langle i_k \rangle$ currents out of I_{dc} solely, regardless of other currents. Amplitude parameter a is introduced to model mutual effects of generated currents, and to make it feasible to generate the set of all phase currents out of I_{dc},which sometimes requires scaling down them by $a < 1$. Finally, modulation index m is introduced to scale down feasible waveforms of $\langle i_k \rangle$ proportionally, when and if needed.

Multi-threshold pulse width modulator

The previously described duty ratio algorithm provides us with the switching frequency average duty cycles. However, the challenge that follows is designing a pulse width modulator circuit that can take these duty ratio values as inputs and generate the gate signal switching sequence at the output. The goal is to ensure that each switch turns off just after an overlap period once the next conducting switch turns on, maintaining a continuous flow of the DC-link current during switch commutation. Two modulators are needed – one for the upper switches and one for the lower switches. In this section, the design of such a pulse width modulator for generating control signals for the upper switches in a three-phase inverter where $n = 3$ is illustrated.

One solution of the modulator is based on the normalized waveforms presented in Fig. 5a: the time variable is normalized to the switching period T_s, while the voltage waveforms are normalized to the sawtooth waveform generator amplitude V_m. In Fig. 5, a sawtooth waveform is compared to $n-1$ threshold levels, which is two in the three-phase case. The levels are set to d_{u1} and $d_{u1} + d_{u2}$, or in general case from d_{u1} up to $\sum_{k=1}^{n-1} d_{uk}$, and provided to the comparators shown in Fig. 5b. This results in auxiliary signals q_{u1} up to $q_{u\,(n-1)}$, the last being q_{u2} in the considered $n = 3$ case. Signals q_{u1} and q_{u2} are also shown in Fig. 5a. These auxiliary signals are fed to the logic circuitry of Fig. 5c which provides the switch gating signals such that $S_{u1} = q_{u1}$, $S_{un} = \neg q_{u\,(n-1)}$, while $S_{uk} = q_{uk} \wedge \neg q_{u\,(k-1)}$ for all of the k values other than 1 and n. Finally, to provide the overlap of gating signals during commutation of the switches, an overlap circuit with a logical structure presented in Fig. 5d is used. The buffer in the circuit of Fig. 5d provides the time delay T_d, which delays falling edge of the gating signal, while the or circuit provides prompt turning on.

Proposed modulator requires one sawtooth or triangular waveform generator, $2\,n-2$ comparators, $2\,n-2$ logic inverters, and $2\,n-4$ logic and circuits with two inputs, as well as $2\,n$ overlap circuits, each consisting of a delay buffer and a logical or circuit with two inputs. The general multi-threshold modulator for an n-phase CSI is illustrated in Fig. 6. It takes the input current references $i_1^*, \ldots, i_n^*$ and generates gate signals for the n-phase CSI. The process begins by dividing the current references by the DC link current I_{dc}. The positive parts of the current references are used to calculate the upper initial duty cycles d_{u0k}, while the negative parts are used to calculate the lower initial duty cycles d_{l0k}. Next, all the initial duty cycles are summed, and their difference to 1 is divided by the number of phases n, and distributed equally between the upper and lower phases. This step produces the final duty cycles d_{uk} and d_{lk}. These final duty cycles are then fed into the multi-threshold modulator, which compares them with the carrier signal to generate the gate signals. It should be noted that when analyzing the general case of an n-phase CSI, the maximum amplitude for sinusoidal currents is limited to its maximum value of $a(n)\,I_{dc}$, where $a(n)$ is defined in Fig. 2. When implementing the method for simulation in a programming language such as Python, it can be organized into distinct modules. For example, one module could handle the calculation of average duty cycles, while the multi-threshold modulator (MTM) could be implemented as a separate module, as it functions identically for both the upper and lower switches, see Fig. 6.

Generalization of the modulator carrier waveform

The carrier waveform shown in Fig. 5a is assumed as a sawtooth one. However, any triangular waveform consisting of two linear segments would provide the same duty ratio values, and the shape of the waveform might be used to optimize the high-frequency part of the generated currents spectra. In that sense, instead of the waveform v_{pwm}/V_m of Fig. 5a that rises from 0 to 1 for $0 \le t/T_s < 1$ and falls back down to zero vertically at $t/T_s = 1$, a waveform with linear rise from 0 to 1 for $0 \le t/T_s < \alpha$ and linear fall from 1 to 0 for $\alpha \le t/T_s < 1$

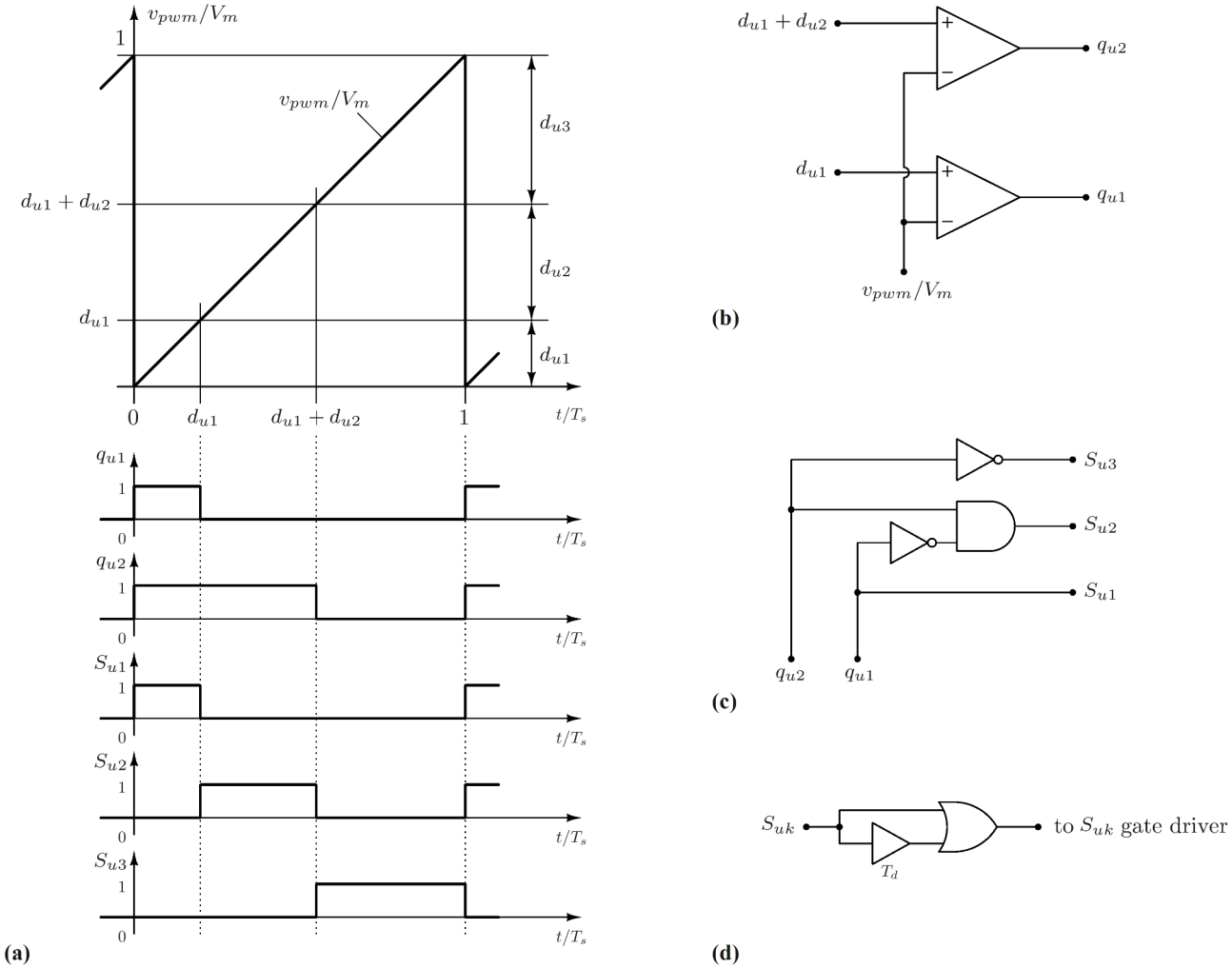

Fig. 5. An example of the proposed multi-threshold pulse width modulator (MTM) for three-phase CSIs: (**a**) the modulator waveforms; (**b**) comparator circuit; (**c**) AND circuit logic for realizing the gate signals; (**d**) overlap circuit.

could be used. The value of α might be used as an additional optimization parameter that affects the high-frequency spectrum.

Furthermore, it is worth to mention that carrier waveforms for the upper set of duty ratio values d_{uk} and the lower set of duty ratio values d_{lk} in the proposed modulator do not have to be the same, neither mutually synchronized.

Simulation results

In this section, the proposed modulation method according to the block diagram shown in Fig. 6a and simulate the power circuit depicted in Fig. 6b is implemented. A simple RL load is used with $R = 11\Omega$ and $L = 200\mu H$. These parameters were chosen to match the load that will be used in the measurements later. The switching frequency is set to 50kHz, and the output filter capacitors are chosen as $C = 1\mu F$. The DC link current is $I_{dc} = 5A$, and the modulation index is maintained at its maximum, $m = 1$. The DC link inductor is $L_{dc} = 1mH$.

The simulation results are presented in Fig. 7. For the 3-phase CSI, the phase currents achieve a maximum amplitude equal to the DC link current. In the case of the 4-phase CSI, the maximum possible amplitude is reduced, as according to Fig. 2, for 4-phase CSI reaching the full amplitude is not possible. The reduction is determined by the parameter a, which is in this case $a(4) = 0.707$, see Fig. 2. It should be noted that this 4-phase (or 4-leg) CSI is frequently analyzed in the literature[8–10,16,18], where proposed modulation methods are often specifically tailored for this 4-phase configuration. Our method covers this 4-phase case as a special case for $n = 4$. Similarly, waveforms for the 5-phase CSI are generated, demonstrating the generality of the proposed method. The maximum phase current amplitude for 5-phase CSI is reduced by $a(5) = 0.618$ with respect to the DC link current.

For all simulations, the same block diagram from Fig. 6a is used for implementation. The only adjustment required for different numbers of phases is the number of comparators in the multi-threshold modulator, which is set to accommodate the respective number of phases.

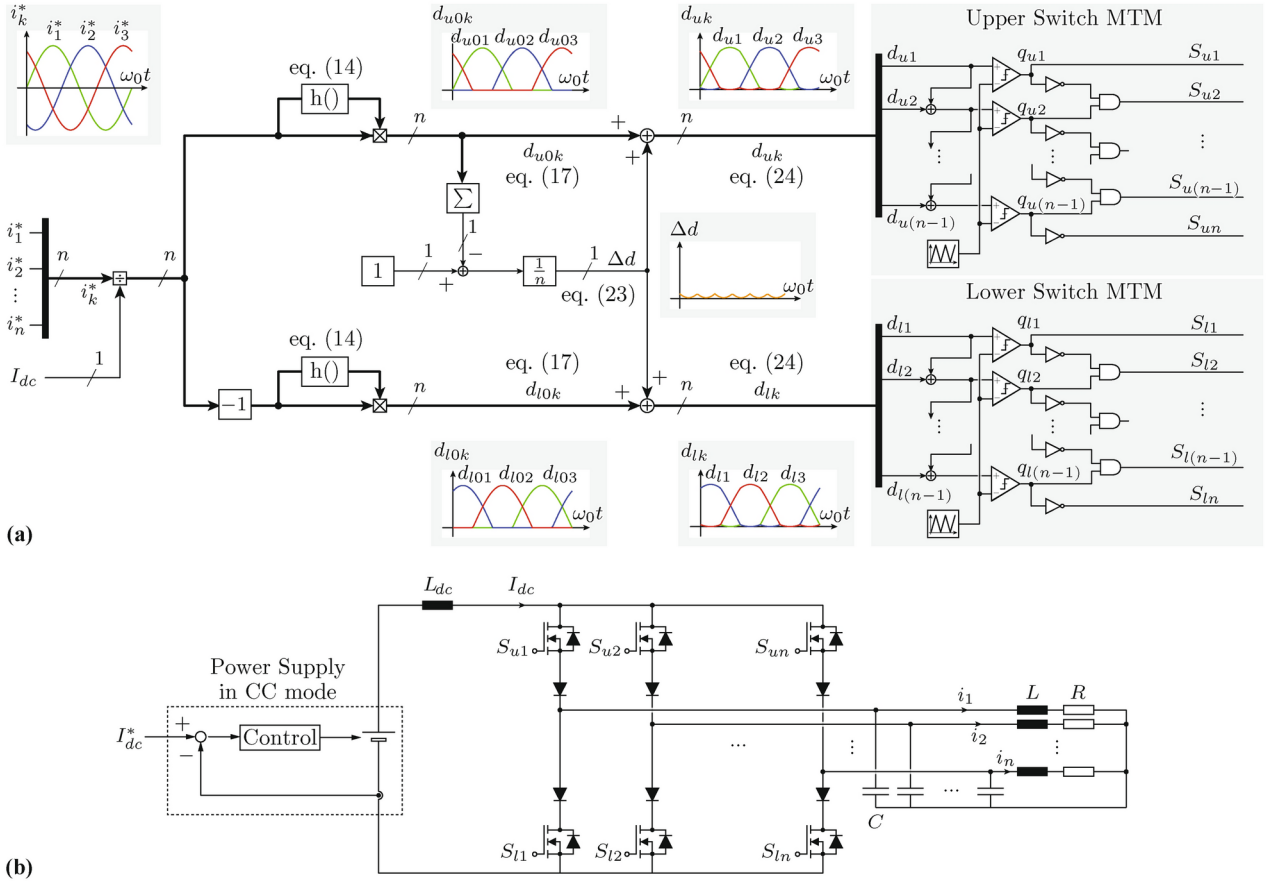

Fig. 6. Entire system diagram: (**a**) Block diagram of the proposed modulation method, illustrating the signal flow with an example waveform of a three-phase sinusoidal reference. The input reference i_k^* is divided by the DC link current I_{dc} and rectified into the duty ratio using the Heaviside function $\mathrm{h}()$, resulting in the upper-side and lower-side duty signals d_{u0k} and d_{lok} respectively. Δd is calculated based on the equation and added to each duty signal before being fed into the multi-threshold PWM modulator (MTM), which generates the gate signals. (**b**) Schematic diagram of the power circuit.

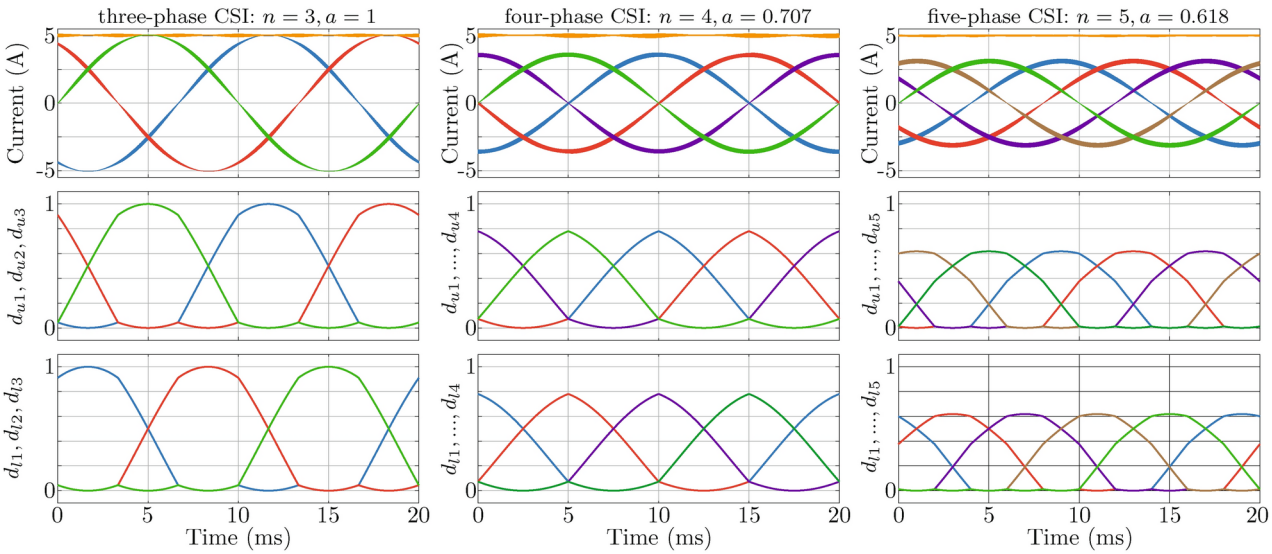

Fig. 7. Simulation results of the proposed modulation method for 3-, 4-, and 5-phase CSIs are presented. Note that for phase counts greater than 3, the maximum amplitude is limited according to $a(n)$. The modulation index for all the simulation examples is $m = 1$.

Experimental results

To verify the proposed modulation method experimentally, a hardware demonstrator was built, as shown in Fig. 8. The schematic is depicted in Fig. 6b, where for the demonstrator $n = 3$. This demonstrator was specifically designed to validate the modulation method rather than to achieve specific power density or efficiency targets. For this purpose, an off-the-shelf DC link inductor of $L_{dc} = 1\text{mH}$ was used. The switching frequency of the CSI demonstrator is set to 50 kHz, which is within the typical range for the selected SiC MOSFETs and diodes. The specifications of these components are provided in the caption of Fig. 8. The output filter capacitors are $C = 1\mu\text{F}$. The modulation method is implemented on PSoC microcontroller.

Multi-threshold modulator verification

The first experiment involved using constant duty cycles to verify the actual gate signals applied to the switches, i.e., the functioning of the multi-threshold modulator (MTM), and to confirm the overlap time. As shown in Fig. 9a, the MTM generates gate signals in a manner that ensures the conduction of switches occurs sequentially. The displayed results correspond to the upper switches, specifically the gate signals for S_{u1} (green), S_{u2} (blue), and S_{u3} (red). Since the MTM for the lower switches operates in the same way, similar waveforms can be observed.

Next, implementation of the overlap time using the digital circuit of Fig. 5d is verified. To implement the necessary delay time T_d, a counter designed to achieve the desired overlap time of $T_d = 41.67\text{ns}$ (a single count of 24MHz FPGA clock) is used. The overlap time was confirmed through measured waveforms, as illustrated in Fig. 9b.

Sinusoidal current waveforms

In this section, the implementation of sinusoidal current references using the proposed modulation method is experimentally verified. Since the hardware demonstrator is a three-phase CSI, the verification is conducted for $n = 3$ (see schematic for general case of phases *n* in Fig. 6b). Implementing the proposed method, as outlined in the block diagram in Fig. 6a, was quick and straightforward.

The first step involves calculating the final duty cycles $d_{u1}, d_{u2}, d_{u3}, d_{l1}, d_{l2}, d_{l3}$ in C within the interrupt routine. The compare levels d_{u1} and $d_{u1} + d_{u2}$ for the upper switches are then fed to the MTM for the upper switches, while d_{l1} and $d_{l1} + d_{l2}$ are fed to the MTM for the lower switches, both of which are implemented in the FPGA of the PSoC mictrocontroller. The DC link current is controlled via a laboratory power supply to $I_{dc} = 5\text{A}$. The sinusoidal waveforms implemented are:

$$
\begin{aligned}
i_1^* &= mI_{dc}\sin(\omega_0 t),\\
i_2^* &= mI_{dc}\sin\left(\omega_0 t - \frac{2\pi}{3}\right),\\
i_3^* &= mI_{dc}\sin\left(\omega_0 t + \frac{2\pi}{3}\right),
\end{aligned}
$$

where $\omega_0 = 2\pi\,50\text{Hz}$,. Measurements were conducted for two different modulation indices. For $m = 0.5$, the experimental results are shown in Fig. 10a, and for $m = 1$, the results are shown in Fig. 10b. In both cases, the modulation method ensures the desired sinusoidal phase currents. When $m = 0.5$, the AC currents have a peak of 2.5A, which aligns with the expected value for this modulation index. The duty cycles d_{u1} and d_{u3}, calculated in the interrupt routine, are provided via the DAC of the PSoC microcontroller and then measured. The DAC's maximum voltage is 2.7V, corresponding to a relative value of 1 for the duty cycles. This result matches expectations and aligns with the simulation shown in Fig. 7.

The waveforms obtained from the simulation for $n = 3$ and $m = 1$ in Fig. 7 match exactly with the measured waveforms in Fig. 10b, fully verifying the simulation results for the three-phase CSI.

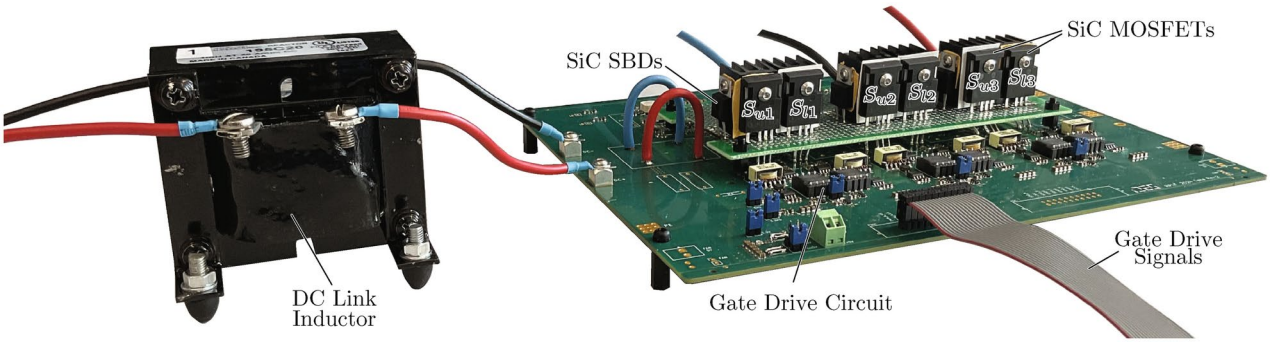

Fig. 8. Hardware demonstrator of the assembled current source inverter (CSI) featuring $650\text{V}/30\text{m}\Omega$ SiC MOSEETs (IMZA65R030M1H, *infineon*), $650\text{V}/10\text{A}$ SiC schottky barrier diodes (IDH10SG60C, *infineon*), and a $1\text{mH}/20\text{A}$ Inductor (195C20, *HAMMOND*).

Fig. 9. Multi-threshold modulator verification, where finally duty cycles are $d_{u1} = 0.3$ (green), $d_{u2} = 0.3$ (blue), and $d_{u3} = 0.4$ (red): (**a**) S_{uk} waveforms. (**b**) Zoomed-in view highlighting the overlap time.

Arbitrary current waveforms

The proposed modulation method for CSIs is capable of generating arbitrary waveforms for the output currents, as described in the section Obtaining the Duty Ratio Values. In this section, the generation of such arbitrary waveforms is experimentally verified. For example, triangular waveforms are selected, which are defined by the following expressions:

$$f(\omega t) = \begin{cases} -\frac{2}{\pi}(\omega_0 t + \pi), & -\pi \leq \omega_0 t < -\frac{\pi}{2}, \\ \frac{2}{\pi}\omega_0 t, & -\frac{\pi}{2} \leq \omega_0 t \leq \frac{\pi}{2}, \\ -\frac{2}{\pi}(\omega_0 t - \pi), & \frac{\pi}{2} \leq \omega_0 t < \pi, \end{cases}$$

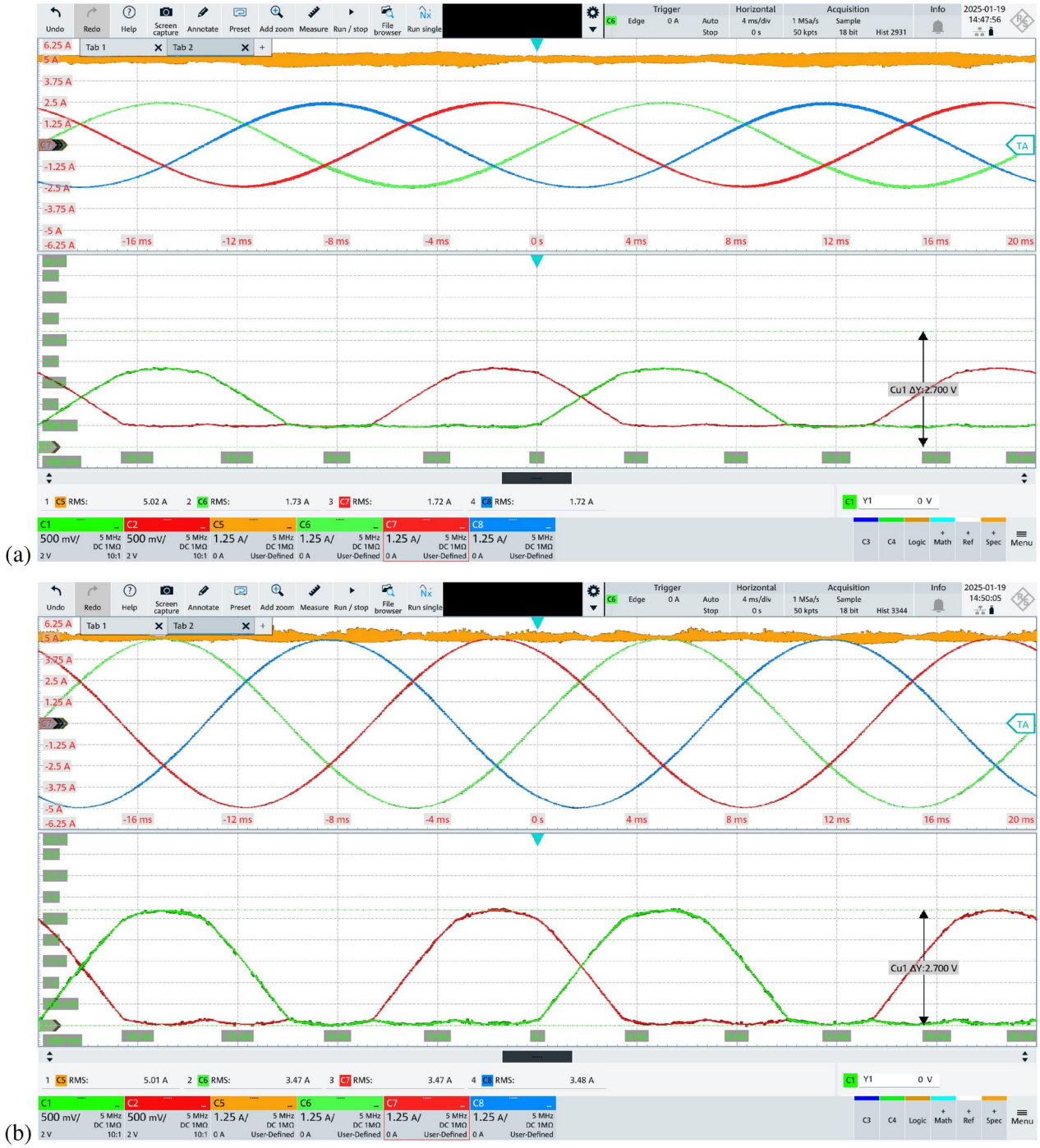

Fig. 10. Experimental measurements for sinusoidal current reference (i_1^*—green, i_2^*—blue, i_3^*—red). Current and final duty cycle waveforms of d_{u1} and d_{u3} for $I_{dc} = 5$A (orange): (**a**) $m = 0.5$. (**b**) $m = 1$.

$$
\begin{aligned}
i_1^* &= mI_{dc}f(\omega_0 t),\\
i_2^* &= -i_1^* - i_3^*,\\
i_3^* &= mI_{dc}f\left(\omega_0 t + \frac{2\pi}{3}\right),
\end{aligned}
$$

where $\omega_0 = 2\pi\,50$Hz. The measurement results are presented in Fig. 11 for $m = 0.4$ and $I_{dc} = 5$A, confirming the successful implementation of the arbitrary waveforms. It should be noted that the DC link current exhibits minor distortions in this case due to the limited current control bandwidth of the power supply. This occurs because, on the DC side of the CSI, arbitrary waveforms introduce a varying impedance to the power supply,

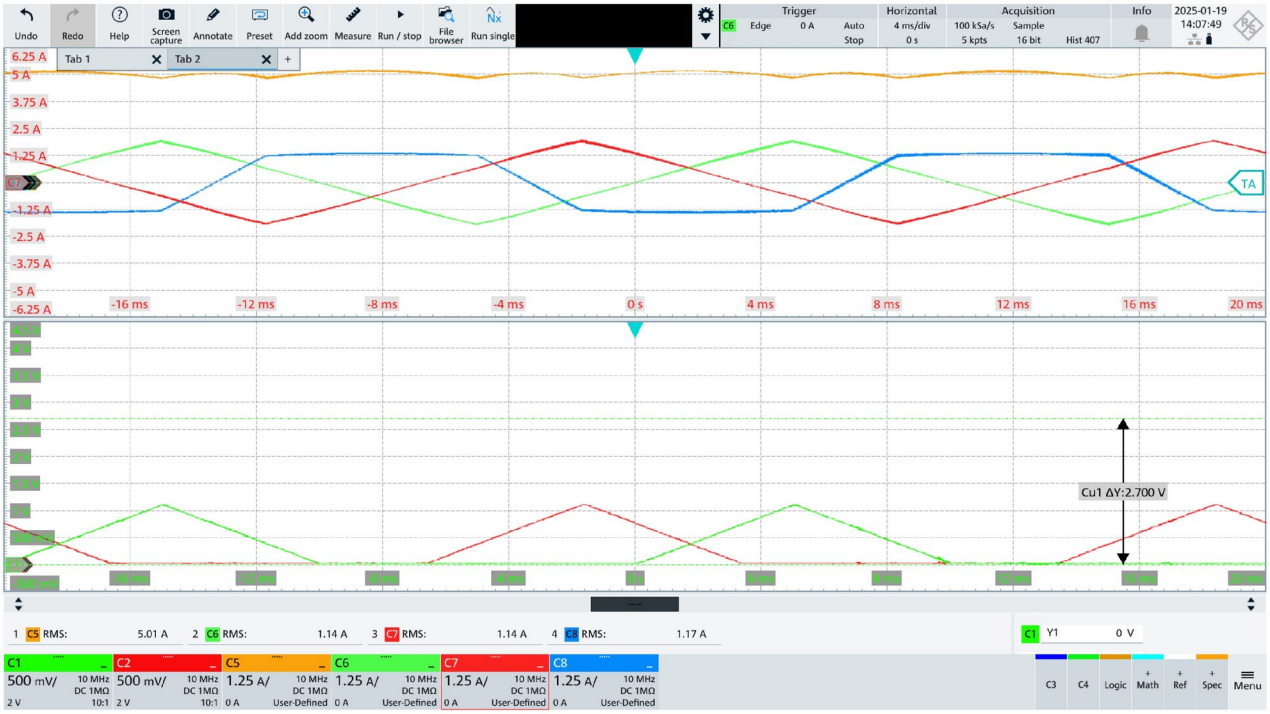

Fig. 11. Triangular current waveforms (i_1^* - green, i_2^* - blue, i_3^* - red) for $I_{dc} = 5\text{A}$ (orange). In the lower part of the oscilloscope screen, d_{u1} (green) and d_{u3} (red) are shown.

unlike sinusoidal currents where the equivalent DC side impedance remains constant. Consequently, the desired shape of the arbitrary waveform dictates the required minimum DC link current control bandwidth.

Conclusion and outlook

In this paper, a pulse width modulation (PWM) technique for current source inverters (CSIs) with an arbitrary number of phases n is proposed. Existing PWM methods for CSIs in the literature typically rely on space vector modulation (SVM) requirements, such as sector detection. In contrast, our method eliminates the need for sector detection, making it a 'pure' PWM approach where the duty cycles are compared to a carrier.

In the first part of the paper, a method to generate switching-frequency-averaged duty cycles for both the *upper* and *lower* switches of the CSI is algebraically derived. Notably, for an n-phase CSI with $2n$ switches, $2n$ duty cycles are computed. Interestingly, $n-1$ degrees of freedom in the calculation of these duty cycles are identified, and the constraints on these degrees of freedom are clarified. This insight is valuable as it allows for optimization of the performance of a CSI, such as minimizing high-frequency ripple in the output capacitors.

Once the $2n$ duty cycles are obtained, they are fed into our specially designed *multi-threshold pulse width modulator*, a novel component for generating gate signals from the calculated duty cycles for CSIs. Regardless of the number of phases, the CSI always requires two such modulators – one for the *upper switches* and one for the *lower switches*. Only that changes with the number of phases is the number of thresholds in the modulator.

To demonstrate the effectiveness and generality of the proposed modulation method, it is first verified through time-domain simulations for 3-, 4-, and 5-phase CSIs. Additionally, to validate the method experimentally, a hardware demonstrator for a 3-phase CSI is built, and the proposed modulation approach is implemented. Experimental measurements were conducted with a DC link current of 5A, showing excellent agreement with the simulation results and fully verifying the method. To further demonstrate the capability of the method to generate arbitrary current waveforms, the measurement results for triangular current waveforms are included.

Our future research will focus on optimizing high-frequency effects and studying overmodulation in CSIs using the proposed modulation method.

Data availability

The data underlying this study's findings are available from the corresponding author upon reasonable request.

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References

1. Van Der Broeck, H. W., Skudelny, H.-C. & Stanke, G. V. Analysis and realization of a pulsewidth modulator based on voltage space vectors. *IEEE Trans. Ind. Appl.* **24**, 142–150 (1988).

2. Ledwich, G. Fixed frequency pwm synthesis. In *Proceedings 14 Annual Conference of Industrial Electronics Society*, vol. 3, 598–602 (IEEE, 1988).
3. Pinewski, P. Understanding space vector modulation. *EDN* **41**, 45–47 (1996).
4. Kolar, J.W., Ertl, H. & Zach, F.C. Analysis of the duality of three phase pwm converters with dc voltage link and dc current link. In *Conference Record of the IEEE Industry Applications Society Annual Meeting,*, 724–737 (IEEE, 1989).
5. Kolar, J. W., Ertl, H. & Zach, F. Quasi-dual modulation of three-phase pwm converters. *IEEE Trans. Ind. Appl.* **29**, 313–319 (1993).
6. Ojo, O. & Vanaparthy, S. Carrier-based discontinuous pwm modulation for current source converters. In *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, vol. 4, 2224–2231 (IEEE, 2004).
7. Ledwich, G. Current source inverter modulation. *IEEE Trans. Power Electron.* **6**, 618–623 (1991).
8. Guo, X., Du, S., Diao, N., Hua, C. & Blaabjerg, F. Three-dimensional space vector modulation for four-leg current-source inverters. *IEEE Trans. Power Electron.* **38**, 13122–13132 (2023).
9. Du, S., Guo, X. & Zhang, P. Generalized modulation of common mode voltage reduction for current source inverter in balanced and unbalanced load cases. *IEEE Trans. Ind. Electron.* (2023).
10. Chen, B., Sun, Y., Xie, S., Liu, Y. & Su, M. High-efficiency modulation scheme for three-level buck four-leg current-source inverter. *IEEE Trans. Power Electron.* (2024).
11. Vaeltman, A. & Holmes, D. G. Charge controlled modulation of a current source inverter. In *IAS'97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*, vol. 2, 1529–1533 (IEEE, 1997).
12. Zmood, D. & Holmes, D. G. A generalized approach to the modulation of current source inverters. In *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196)*, vol. 1, 739–745 (IEEE, 1998).
13. Zmood, D. N. & Holmes, D. G. Improved voltage regulation for current-source inverters. *IEEE Trans. Ind. Appl.* **37**, 1028–1036 (2001).
14. Holmes, D. G. & Lipo, T. A. *Pulse width modulation for power converters: Principles and practice*, vol. 18 (John Wiley & Sons, 2003).
15. Elgenedy, M. A., Elserougi, A. A., Abdel-Khalik, A. S., Massoud, A. M. & Ahmed, S. A space vector pwm scheme for five-phase current-source converters. *IEEE Trans. Ind. Electron.* **63**, 562–573 (2015).
16. Guo, X., Xu, D. & Wu, B. Four-leg current-source inverter with a new space vector modulation for common-mode voltage suppression. *IEEE Trans. Ind. Electron.* **62**, 6003–6007 (2015).
17. Taha, W., Azer, P., Callegaro, A. D. & Emadi, A. Multiphase traction inverters: State-of-the-art review and future trends. *IEEE Access* **10**, 4580–4599 (2022).
18. Du, S. & Guo, X. A simplified space vector modulation in abc coordinate for four-leg current source inverters. *IEEE Trans. Ind. Electron.* (2024).
19. Choi, N.-S., Lee, K.-W. & Han, B.-M. A novel carrier based pwm for current source converter. In *Proceedings of The 7th International Power Electronics and Motion Control Conference*, vol. 3, 1945–1950 (IEEE, 2012).
20. Xiong, W., Yi, S., Lin, J., Sun, Y. & Su, M. Algebraic modulation scheme for current source converter. *IEEE Trans. Power Electron.* (2023).
21. Espinoza, J. R. & Joos, G. Current-source converter on-line pattern generator switching frequency minimization. *IEEE Trans. Ind. Electron.* **44**, 198–206 (1997).
22. Mirić, S., Borović, U. & Pejović, P. Modulation in voltage source inverters: An algebraic approach. *IEEE Access* (2024).

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Author contributions

All authors contributed equally to the conception, design, and execution of the research. They were equally involved in the analysis and interpretation of the data, as well as the writing and revision of the manuscript. All authors reviewed and approved the final version of the manuscript for submission.

Additional information

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